III B.C.A - V SEMESTER

MICROPROCESSORS AND MICROCONTROLLERS

UNIT I :

8085 Microprocessor :

Introduction to Microcprocessor
8085 architecture and its operations
8085 Pin description
8085 Instruction set and Classification
8085 Addressing Modes.

UNIT 1:

1. INTRODUCTION TO MICROPROCESSOR

Definition: Microprocessor

"Microprocessor is a Programmable integrated device that computing and decision making Capability..

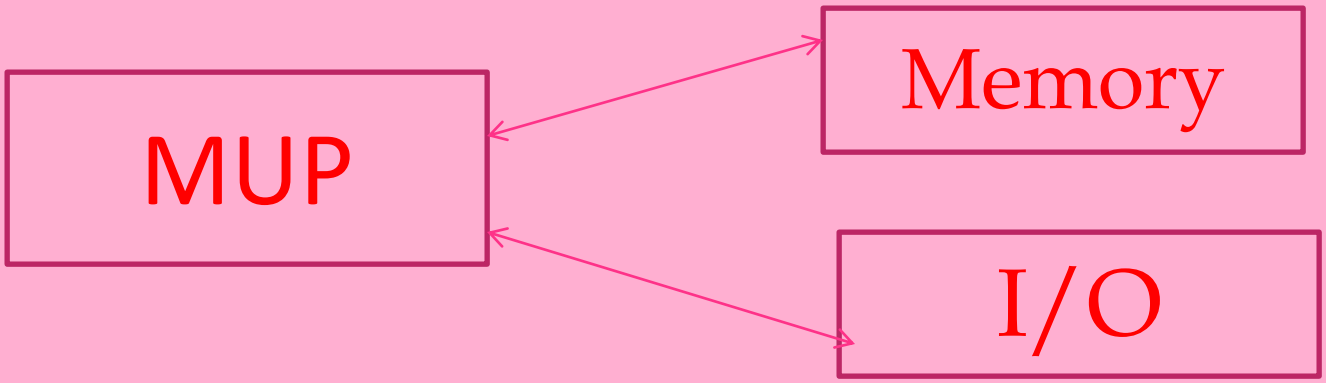
Microprocessor Unit:

Programmable machine as three Components:

- ❖MUP
- ❖Memory
- ❖I/O

Three Components worked together to perform a task.

1. Physical Components – Hardware
2. Set of Instruction "Program"
3. Group of Program "software"



Binary Digit:

- MUP operated 0,1 (Bits, Binary)
- Each MUP recognizes group of bits
  E.g: 8 Bit , 16 Bit, 32 Bit

Memory :

- Pages –Note book
- Fixed Numbers – line

Input / Output :

- Keyboard – Input
- Monitor – Output

Microcomputer

A computer that is designed using MUP as its CPU

- MUP
- Memory
- Input
- Output

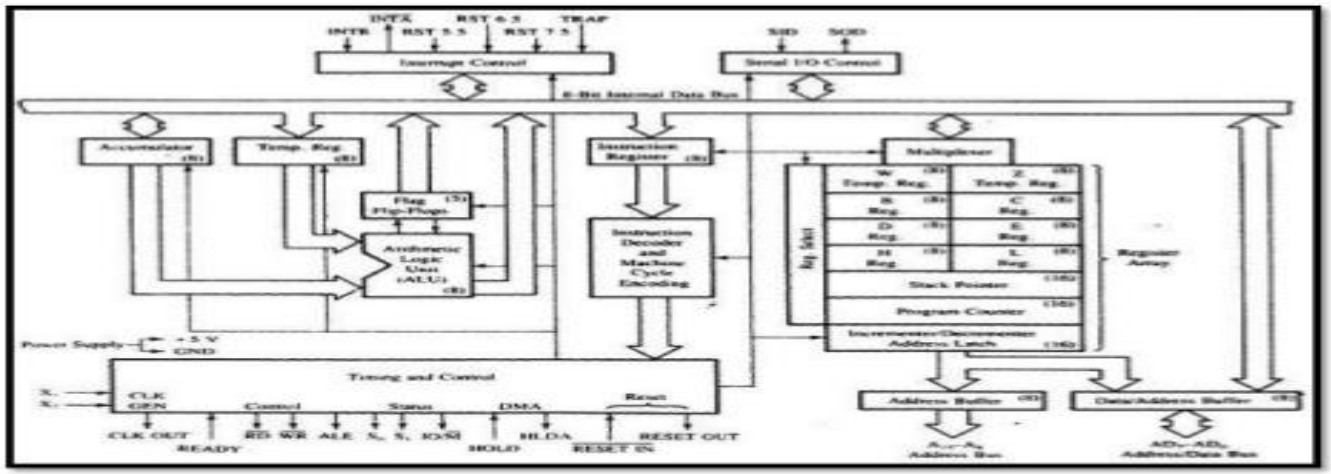
Difference Models of Microprocessor

8085 , 8086 , 8088, 80386 , 80486

2. Microprocosser Architecute & its Operations

MUP is a Programmable device designed with registers, Flip flops, & timing Elements.

Internal Architecture of 8085 Microprocessor



All function classified 3 categories

1.Microprocessor initiated operations.
2.Internal data operations.
3.Peripheral (Externally) functions.

1. Microprocessor initiated operations:

4 operations

- **Memory Read**
- **Memory Write**
- **I/O Read**
- **I/O Write**

Communications --- MUP to Memory ,
MUP to I/O
Buses - Address Bus, Data Bus, Control Bus

1. Address Bus

- **16 lines unidirectional**
- **A0 to A15**

2.Data Bus

- **8 lines Bidirectional**
- **Do to D7**

3.Control Bus

- **Signal for operations**

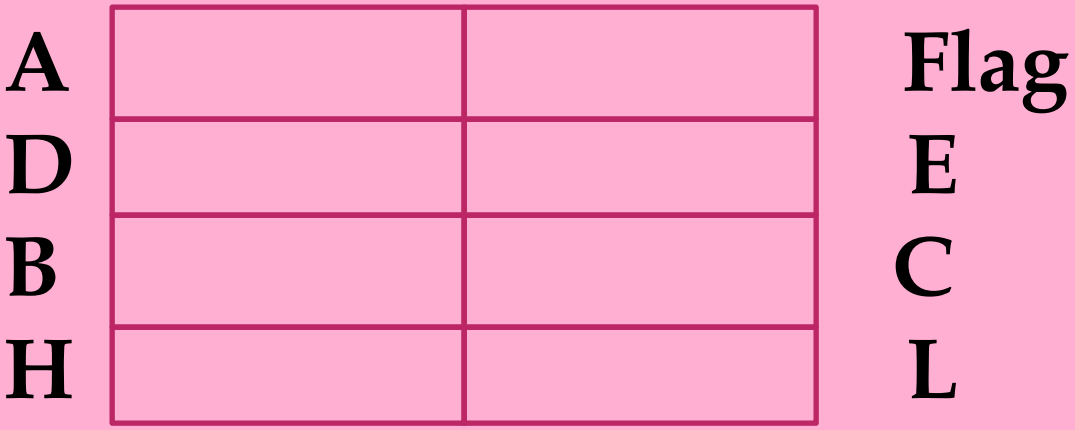
2. Internal Data Operations

- 8 Bit data
- Perform Arithmetic Operations
- Test Conditions
- Sequence of Instructions
- Store data in Memory Locations

Requirements : Registers
Timing Element

Registers :

A, B, C, D, E, H, L (8 Bits)



A- Accumulator

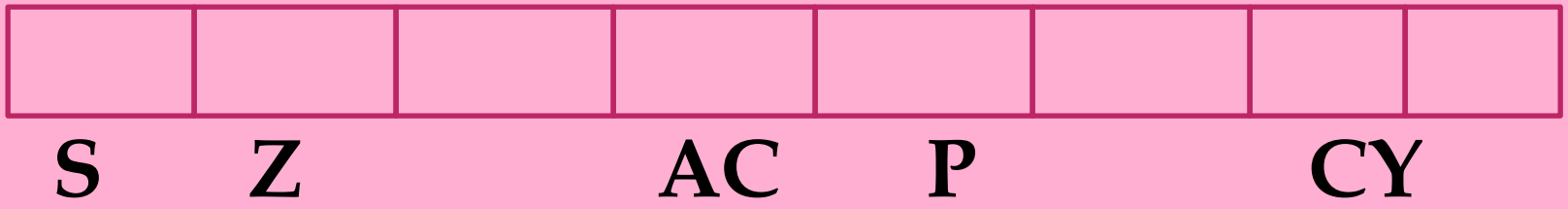
Others – General Purpose Register.

(B ,C ,D ,E ,H ,L)

16 Bit Register Pair : BC , DE, HL

Program Counter & Stack Register

Flag:



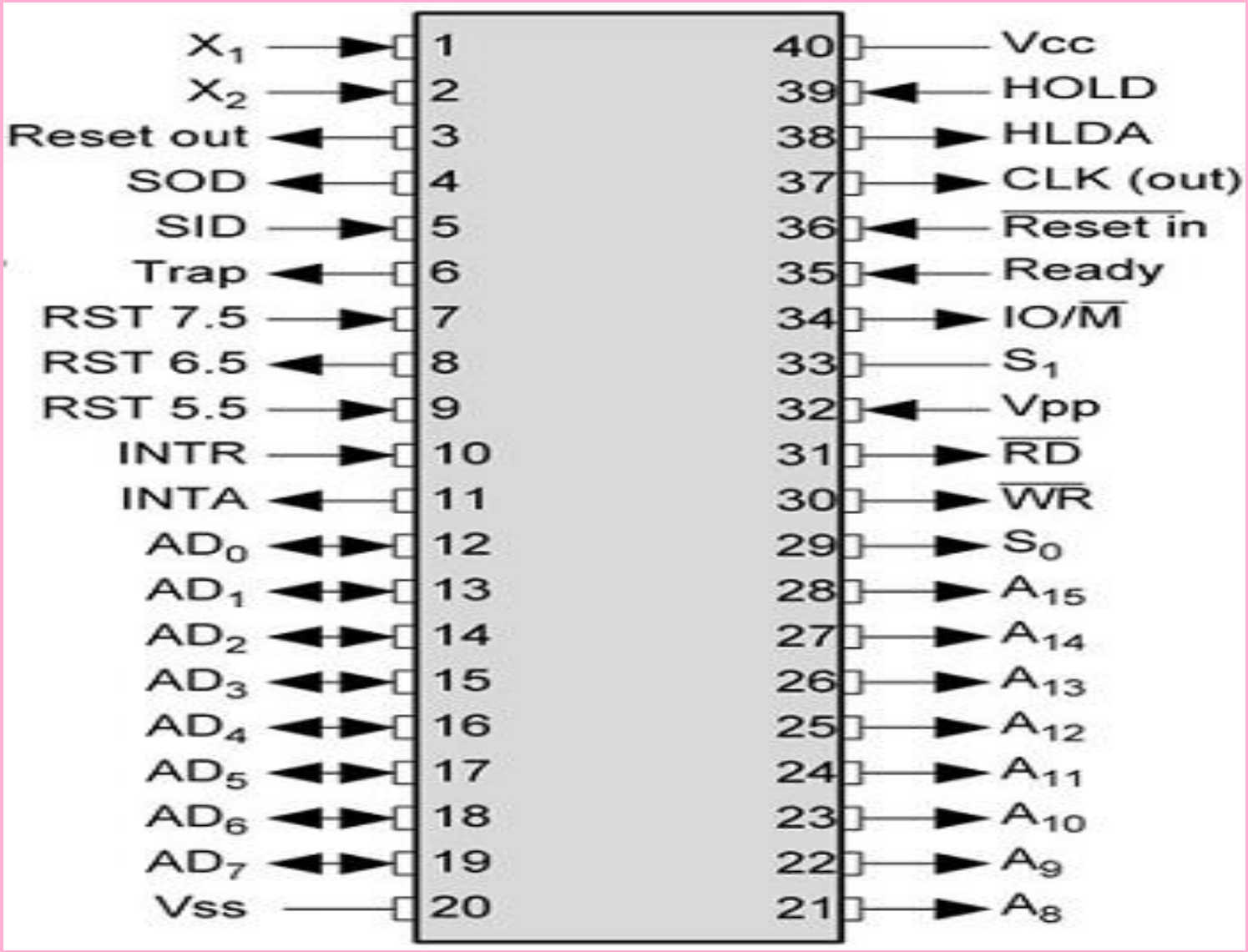
S - Sign
Z - Zero
AC – Auxillary Carry
P - Parity
CY - Carry

3. Peripheral (External) Operation

Reset - Cleared
Interrupt – Normal Interuupt (Program)
Ready – Wait
Hold - Activation

3. 8085 PIN Description

40 Pins, +5v , 3Mhz



All signals classified in to 6 groups

1. **Address Bus**
2. **Data Bus**
3. **Control & Status Signal**
4. **Power supply & Frequency Signal**
5. **External initiated Signal**
6. **Serial I/O signal**

1. Address Bus
   16 lines unidirectional

2. Data Bus
   8 lines – Bidirectional
   Multiplexed mode

3 . Control & Status Signal
   a. Control Signal : RD & WR
   b. Status Signal : ALE, S0,S1 IO/ M

S1	S0	IO/M	Function
1	0	0	Memory Read
0	1	0	Memory Write
1	0	1	I/O – Read
0	1	1	I/O - Write

4. Power supply & Frequncy Signal

A: Power Supply

VCC : +5V , VSS : Ground

B: Frequency Signal :

X1 & X2 : Crystal
CLK : Clock

5. External initiated Signal

INTR - Interrupt
INTA - Interrupt ACK
TRAP
RST 7.5
RST 6.5
RST 5.5
HOLD
HLDA
RESET IN, RESET OUT
READY

5. Serial I / O Signal

SID	-	Serial Input Data
SOD	-	Serial Output Data

4. 8085 INSTRUCTIONS SET AND CLASSIFICATION

8085 - 5 functional Parts

1. Data Transfer Instructions
2. Arithmetic Group Instructions
3. Logic Group Instructions
4. Branch Group Instructions
5. Stack, I/O, Machine Control group Instructions

1. Data Transfer Instructions

- Group of Instructions Move data
  - Register to Register
  - Register to Memory
  - Memory to Register
- Copies Sources to Destination
- Copies Remains same after Transfer
- Flag Not affected

2.Arithmetic Group Instructions

- Add, Sub, Mul, Div
- Increment , Decrement
- Accumulator used
- Flag affected (Updated)

3. Logic Group Instructions

- AND, OR,XOR , Complement
- Accumulator used
- Flag affected (Updated)

4. Branch Group Instructions

- Alter Normal Flow
- Unconditional Jump
- Conditional Jump
- Flag not affected

5. Stack, I/O Machine Control Group Instructions

- Stack Instrcution
- I/O Instructions
- Machine Control Instructions

1. Data Transfer Instructions

1. **Mov r1, r2** : Move Register to Register
2. **Mov r, m** : Move Memory to Register
3. **Mov m,r** : Move Register to Memory

4. **MVI r, data (8 bits)** : Move immediate data to Register
5. **MVI m, data(8 bits)** : Move immediate data to Memory

6. **LDA address (16 Bits) :**

Load Accumulator Direct

7 **STA address (16 Bits) :**

Store Accumulator Direct

8. **LXI rp data (16 Bits) : Load** immediate data to Register Pair

9. **LDAX rp :**

Load Accumulator Indirect

10. **STAX rp :**

Store Accumulator Indirect

11. LHLD address (16 Bits) :

Load H & L Direct

12. SHLD address (16 Bits) :

Store H & L Direct

13. XCHG :

Exchange between HL & DE

2. Arithmetic Group Instructions

a. *Addition Instruction:*

1. ADD r : Add Register with Accumulator
2. ADD m : Add memory with Accumulator
3. ADI data(8 Bit) : Add immediate data with accumulator
4. ADC r : Add Register & carry with Accumulator
5. ADC m : Add Memory & carry with Accumulator
6. ACI data (8 Bit) : Add Immediate data & carry with Accumulator

b. Subtraction Instruction:

1. **SUB r : Sub Register with Accumulator**
2. **SUB m : Sub memory with Accumulator**
3. **SUI data (8 Bit) : Sub immediate data with accumulator**
4. **SBB r : Sub Register & Borrow with Accumulator**
5. **SBB m : Sub Memory & Borrow with Accumulator**
6. **SBI data(8 Bit) : Sub Immediate data & Borrow with Accumulator**

C. Increment / Decrement Instruction:

1. **INR r** : **Increment Register**
2. **INR m** : **Increment Memory**
3. **DCR r** : **Decrement Register**
4. **DCR M** : **Decrement Memory**
5. **INX rp** : **Increment Register Pair**
6. **DCX rp** : **Decrement Register Pair**
7. **DAD** : **Add Register pair to HL**
8. **DAA** : **Decimal adjust Accumulator**

Unit 2

Chapter II : 8085 Programming

1. *Writing assembly level programs*
2. Multi Byte Addition
3. Multi Byte Subtraction
4. BCD Addition
5. BCD Subtraction
6. BCD Multiplication
7. BCD Division
8. BCD To Binary Conversion(decimal to HEX)

9 Binary To BCD Conversion(HEX To decimal)

10. ASCII to Binary Conversion
11. Binary to ASCII Conversion
12. ASCII To BCD
13. BCD To ASCII

1. Writing assembly level programs

Algorithm:
Step !: Read Problem
Step 2: Break
Step 3: Flowchart
Step 4: Translate Flowchart to Mnemonics
Step 5: Mnemonics to Machine Code
Step 6: Machine Code – Execution
Step 7: Start Troubleshooting.

Eg: *ADD Two 8 Bit numbers*

1. *Break : Laod, Add, Store*
2. *Flowchart*

3. Translate Mnemonics

Task 1 : MVI A 20
MVI B 40
Task 2: ADD B
Task 3: STA 4200

4. Mnemonics to Machine Code

Mnemonics	*Machine Code*
MVI A 20	*3E 20*
MVI B 40	*06 40*
ADD B	*80*
STA 4200	*32 00 42*
HLT	*76*

2. *Multi Byte Addition (16 Bit, 32 Bit, 64 Bit)*

Algorithm:

Program :

```
    XRA  A
    MVI C 02
    LXI  H  2050
    LXI  D 2060

HERE :  LDAX   D
        ADC  M
        MOV   M,A
        INX  H
        INX  D
        DCR   C
        JNZ   HERE
        HLT
```

EXAMPLE

Input 1:	*12*	*34*
Input 2:	*AB*	*CD*
SUM	*BE*	*01*

Input	*2050 :*	*34*
	2051:	*12*
Input 2 :	*2060:*	*CD*
	2061:	*AB*
Sum:	*2050:*	*01*
	2051	*BE*

2. *Multi Byte Subtraction (16 Bit, 32 Bit, 64 Bit)*

Algorithm:

Program :

```
    XRA  A
    MVI C 02
    LXI  H  2050
    LXI  D 2060

HERE :  LDAX   D
        SBB  M
        MOV   M,A
        INX  H
        INX  D
        DCR   C
        JNZ   HERE
        HLT
```

EXAMPLE

Input 1:	*57*	*DD*
Input 2:	*AB*	*CD*
Difference	*53*	*F0*

Input	*2050 :*	*DD*
	2051:	*57*
Input 2 :	*2060:*	*CD*
	2061:	*AB*
Difference:	*2050:*	*53*
	2051:	*F0*

4. BCD Addition (8 Bit Addition) *(99 less then or equal)*

- *The Maximum two digit (8 Bit) is 99*
- *DAA used after increment or Addition*

Algorithm:

Program :

```
LDA 2050
MVI  B,A
LDA 2051
ADD B
DAA
STA 2052
HLT
```

EXAMPLE

Input	*2050 :*	*25*
	2051:	*56*
Sum :	*2052:*	*81*

.

5. BCD subtraction (8 Bit subtraction) (99 less then or equal)

Algorithm:

Program :

```
LDA 2050
MVI  B,A
LDA 2051
MOV C,A
MVI   A,99
SUB C
INR A
ADD B
 DAA
 STA   2052
  HLT
```

Example:

Minuend = 85

Subtrahand = 39

9' s Complement of 39 = 99-39 = 60

10' s Complement of 39

(9's Complement + 1) = 60 +1 = 61

Therefore : 85

61

1 46

omitting the carry, we get the result as 46

INPUT : 2050 : 85 ; 2051: 39

Difference : 2052: 46

.

7. BCD Division (8 Bit Division) (99 less then or equal)

Algorithm:

Program :

```
        LDA 2050
        MOV  B,A
        LDA 2051
        MOV E,A
        MVI C,99
AGAIN: XRA   A
       MOV A,C
         INR A
        DAA
         MOV C,A
         CALL BCDSUB
         JC AGAIN
         ADD B
         DAA
          STA 2053
         MOV A,C
          STA 2052
         HLT
```

BCD SUB:

```
XRA A
MVI A, 99
SUB B
INR A
ADD E
DAA
MOV E,A
RET
```

INPUT :

2050 : 3

2051 : 21

OUTPUT

2053 : 0 (Remainder)

2052: 7 (Quotient)

8. BCD to Binary (Decimal to HEX)

EXAMPLE: (98) 10 = (1001 1000) and is equal to $(62)_H$ (0110 0010)

Algorithm:

Program :

```
        LDA 2050
        MOV  B,A
        ANI  OF
        MOV  C,A
        MOV A, B
        MVI  F0
        RRC
        RRC
         RRC
         RRC
        MOV  D, A
        XRA A
        MOV  E, 0A
LOOP:  ADD D
     .   DCR E
         JNZ LOOP
         ADD C
         STA 2051
          HLT
```

INPUT 2050 : 98 **OUTPUT** 2051 : 62

9. Binary to BCD (HEX to Decimal)

EXAMPLE: $(FE)_{16} = (254)_{10}$

Algorithm:

Program :

```
        LDA 2050
        LXI H 2051
        MVI B 64
        CALL  DIVIN
       MVI B , 0A
        CALL DIVIN
        MOV M,A
        HLT
DIVN :
        MVI M FF
   LOOP : INR M
          SUB B
          JNZ LOOP
          ADD B
          INX H
          RET
```

INPUT : 2050: FE ; OUTPUT: 2051: 02, 2052: 05, 2053: 04

Binary	Hex	ASCII	
0000	0	011 0000	30_H
0001	1	011 0001	31_H
0010	2	011 0010	32_H
0011	3	011 0011	33_H
0100	4	011 0100	34_H
0101	5	011 0101	35_H
0110	6	011 0110	36_H
0111	7	011 0111	37_H
1000	8	011 1000	38_H
1001	9	011 1001	39_H
1010	A	100 0001	41_H
1011	B	100 0010	42_H
1100	C	100 0011	43_H
1101	D	100 0100	44_H
1110	E	100 0101	45_H
1111	F	100 0110	46_H

10. Binary to ASCII

0 to 9 add 30
A to F add 30 & 7

Algorithm:

Program :

```
        LDA 2050
        CPI  0A
        JC  SKIP 7
        ADI  07
SKIP 7 :
        ADI 30
        STA  2051
        HLT
```

INPUT : 2050: 0B

OUTPUT: 2051: 42

11. ASCII to BINARY

0 to 9 SUB 30
A to F SUB 30 & 7

Algorithm:

Program :

```
        LDA 2050
        CPI  0A
        JC  SKIP 7
        SUI  07
SKIP 7 :

        SUI 30
        STA  2051
        HLT
```

INPUT : 2050: 42

OUTPUT: 2051: 0B

12. BCD TO ASCII (0 TO 9)

Algorithm:

Program :

```
LDA 2050
ADI  30
STA  2051
HLT
```

INPUT : 2050: 08

OUTPUT: 2051: 38

12. ASCII TO BCD (30 TO 39)

Algorithm:

Program :

```
LDA 2050
SUI  30
STA  2051
HLT
```

INPUT : 2050: 38

OUTPUT: 2051: 08

Unit - 3

Chapter III :

INTEL 8255A PROGRAMMABLE PERIPHERAL INTERFACE [8255 PPI]

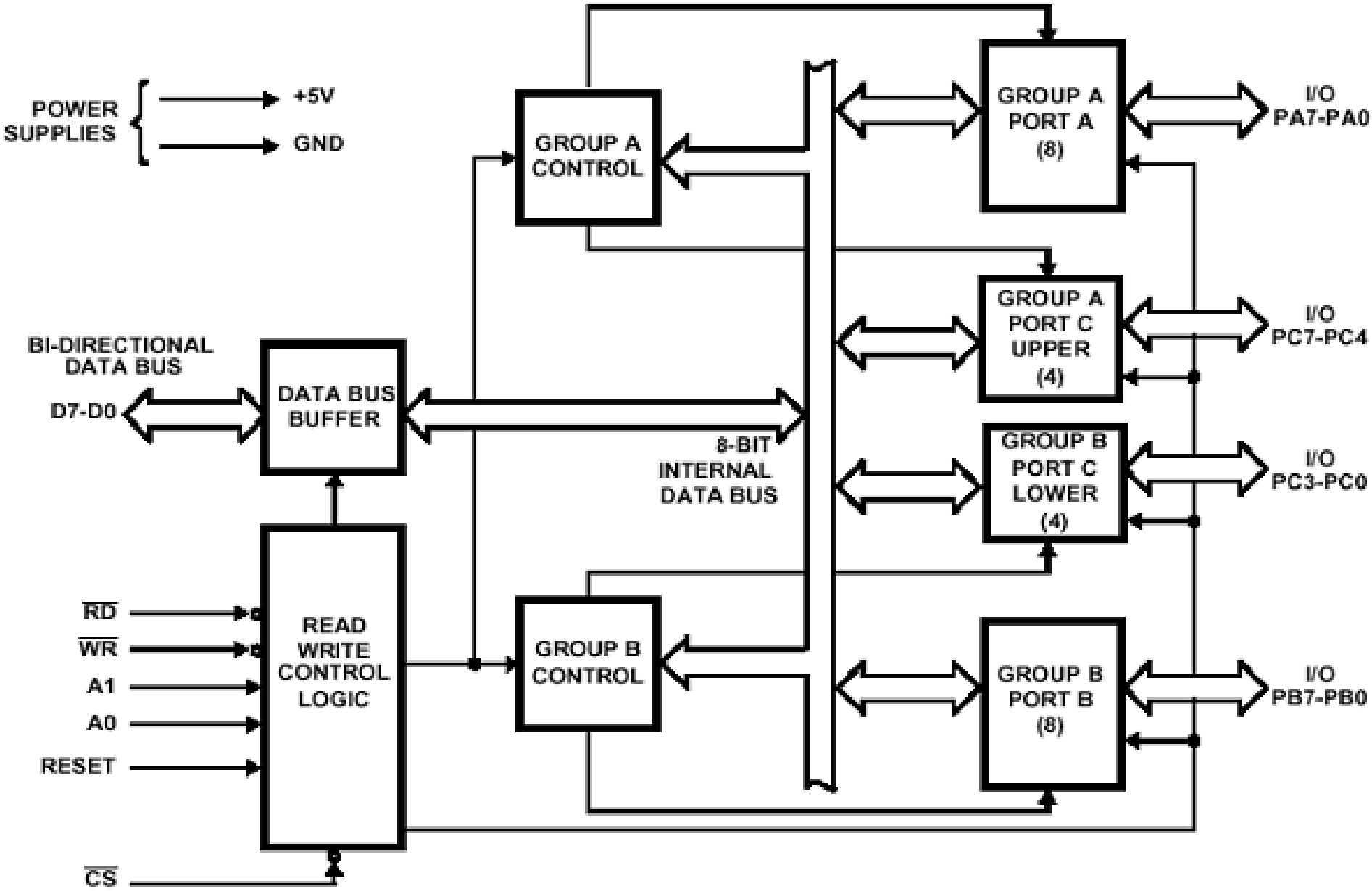
1. Features of 8255A - (5 Marks)
2. Block Diagram of intel 8255A - (10 Marks)
3. Operating Modes & controls words of 8255A – (5 Marks)
4. Programming Examples. (5 Marks)
5. Interfacing Switches & LEDs - (10 Marks)
   (a) Example Program (5 Marks)
6. Interfacing Seven Segment Displays – (10 or 5 Marks)
7. Traffic Light Control – (10 Marks)

1. FEATURES OF 8255A - (5 Marks)

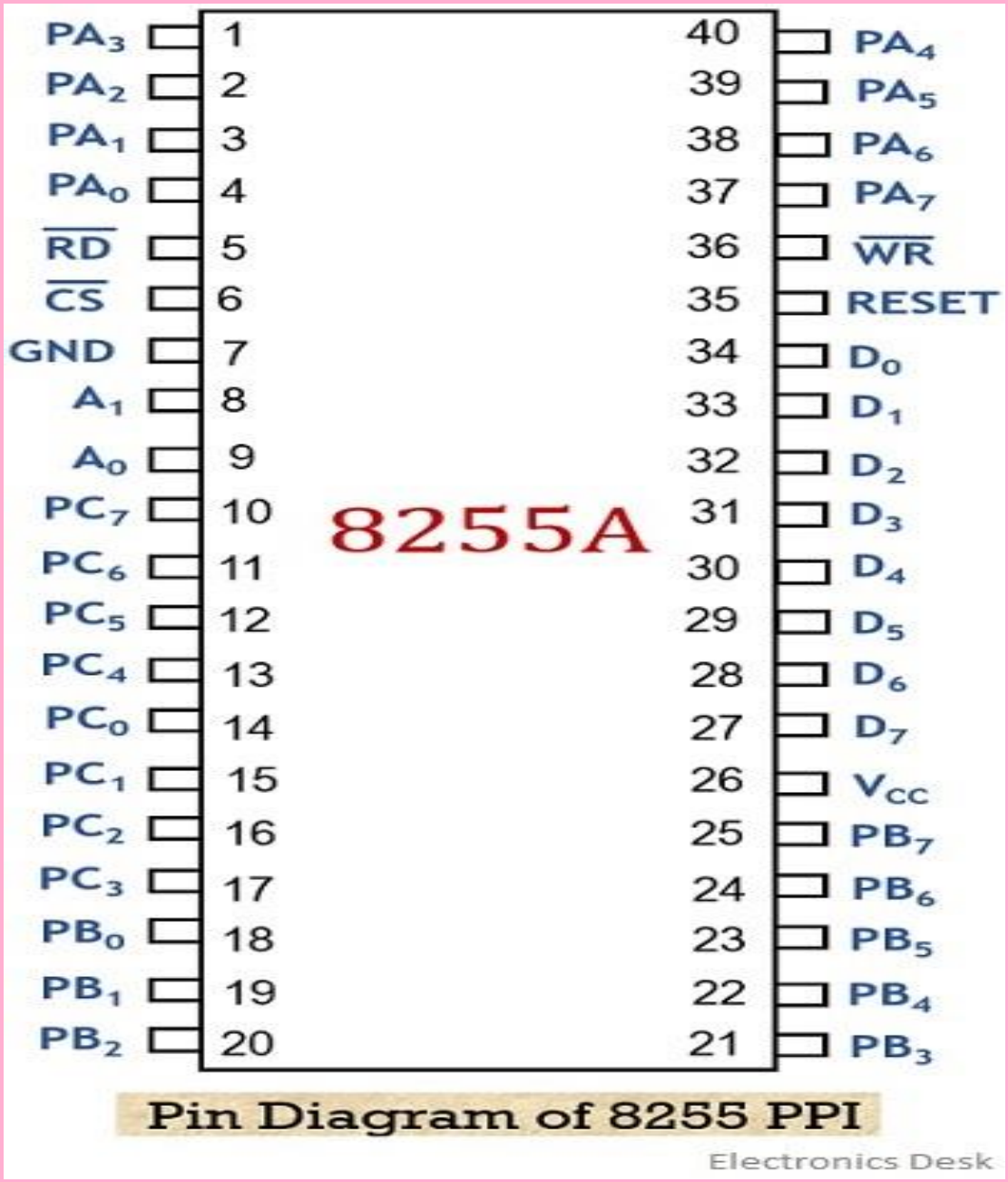
- 3 - 8 Bit Port or Register (A, B, C) connected by pins
- Port C divided into 2 Groups
  - Port C upper [PCU]
  - Port C lower [PCL]
  - Each 4 Bit Pattern
  - Port C Set / Reset individually
- All Ports simple I/O or Handahake I/O
- Port A & Port CU [Group A] – GA
- Port B & Port CL [Group B] - GB

2. Block Diagram of 8255A

Dig 1 : Internal Block Diagram of 8255A



Dig 2 : Pin Diagram of 8255A



- A,B,C - GA & GB

- Control Register – Contents decides operating Modes Simultaneously

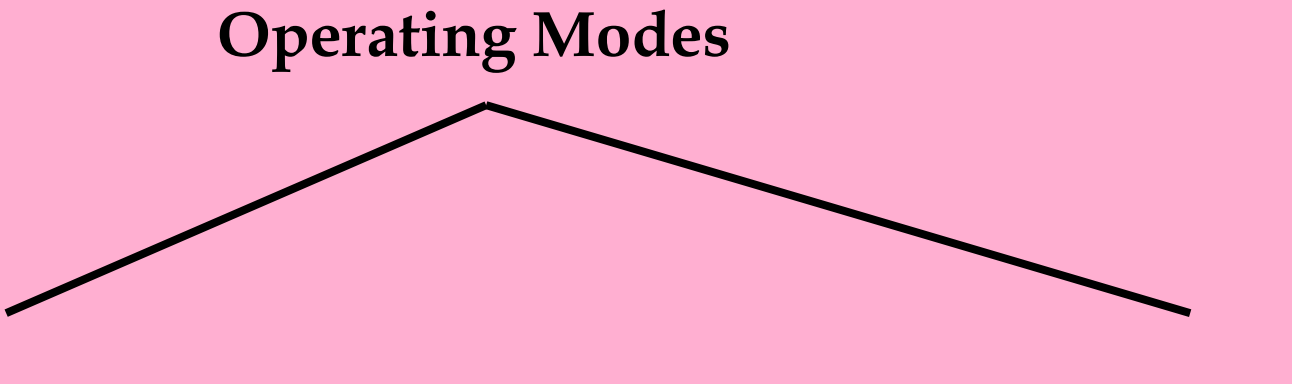
A1	A0	Register Selected
0	0	Port A
0	1	Port B
1	0	Port C
1	1	Control Register

- 24 Pins
- D0 – D7 – Data Lines interfacing 8085 Data Lines
- A0 & A1 - Select Register
- RD/ WR Signals
- CS – Chip Select
- RESET – Interfacing with RESET OUT (8085)
- VCC – Power Supply ;
- GND – Ground Signal

3. OPERATING MODES AND CONTROL WORDS of 8255A

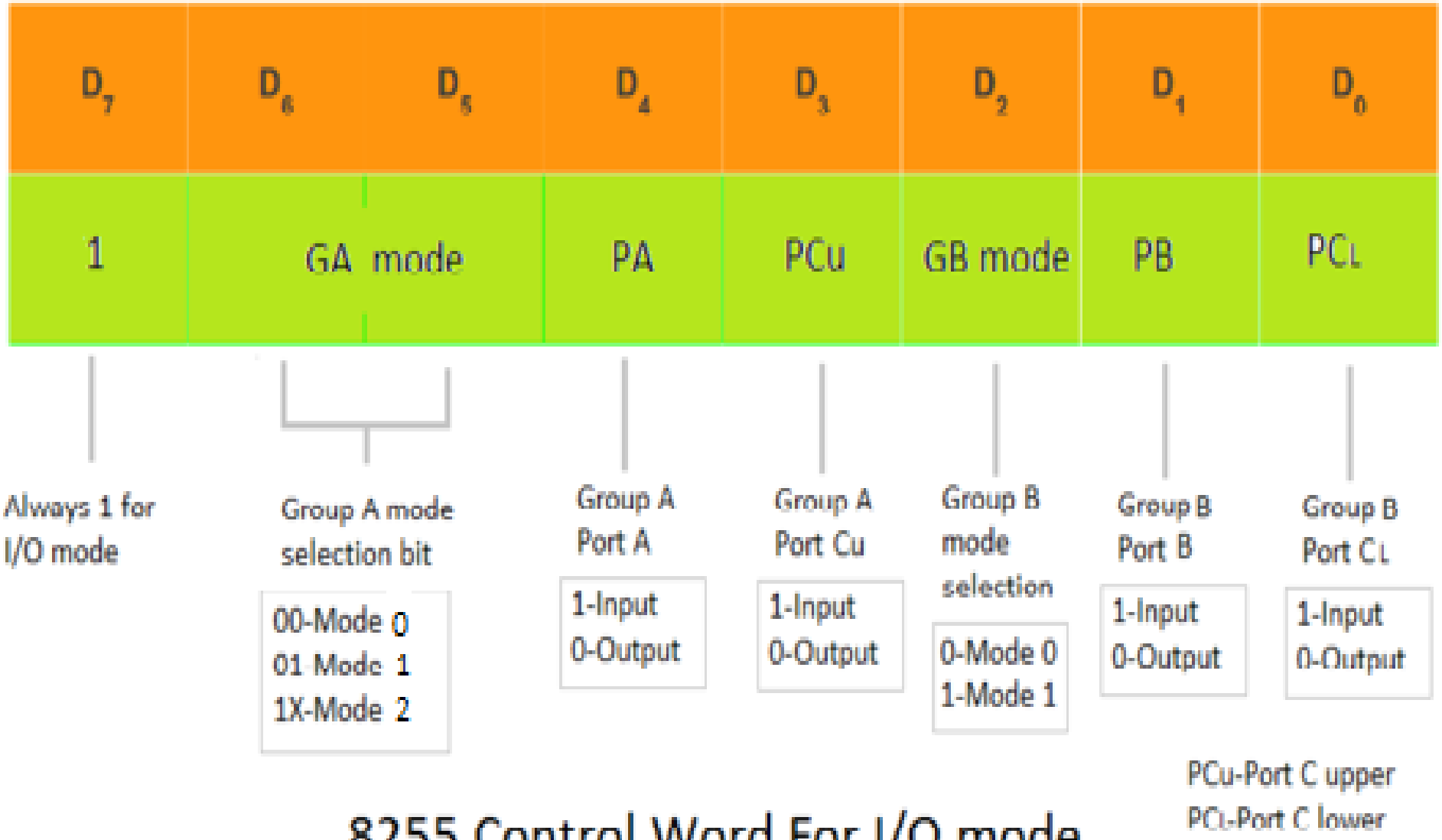
- Control Register - Control Words – Different Configuration
- Basic Operating Modes :

1. I/O Mode
2. BSR Mode



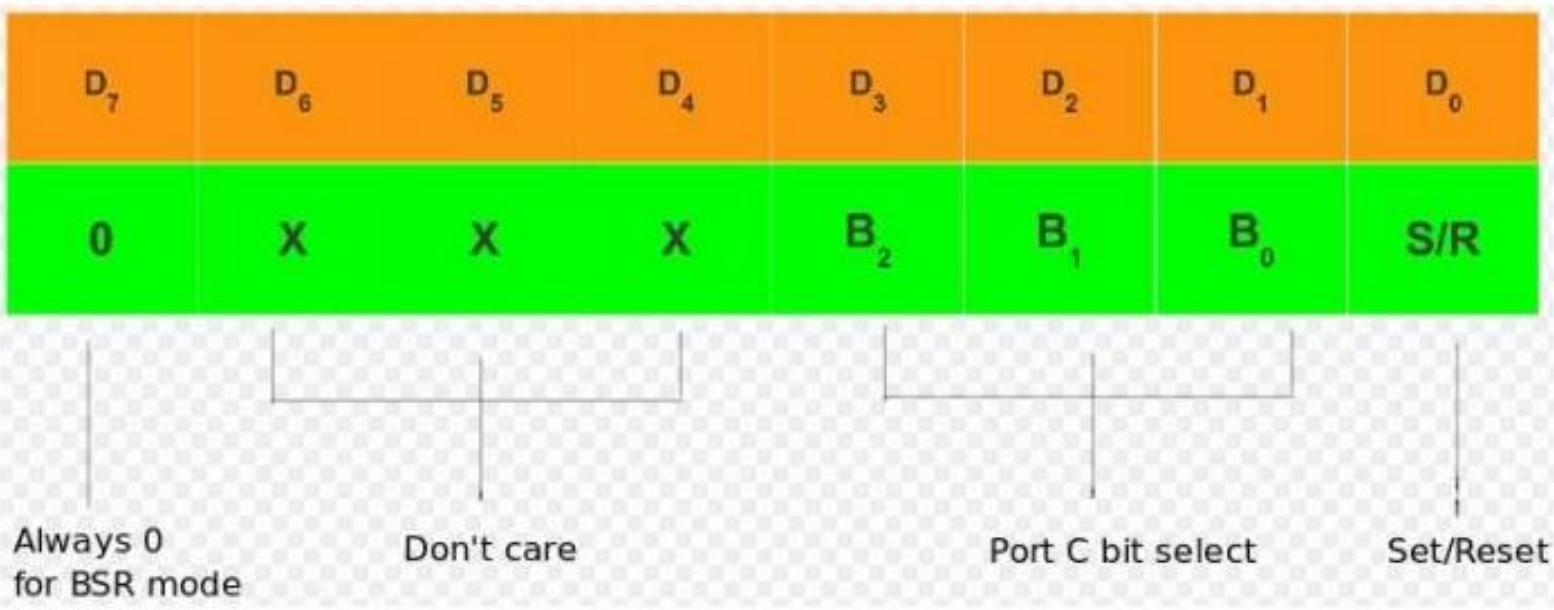
- **Mode 0 : Basic I/O**
  - Applicable to Port A,B,C
- **Mode 1 : Handshake I/O**
  - Applicable to Group A & B (Handshake)
- **Mode 2 : Bidirectional I/O**
  - Applicable to Group A Only

A. I/O Mode Control word Format :



8255 Control Word For I/O mode

A. BSR MODE CONTROL WORD FORMAT :



Control Register format in BSR mode

4. Programming Examples :

a. **Configure Ports of 8255A given below**

Port A = Input
Port B = Output
PCU = Output
PCL = Input

Assume 4 Register located 40 -43 .

Solution:

The Control Format given a conditions as given below

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	0	0	0	1

```
MVI  A 91
OUT 43
```

b. Find the data direction & mode of operation in 8255 of control word is A0. The Control Word Bit Pattern is given below,

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	0	0	0	0	0

.

Solution:

D6, D5 = 0,1 - Mode 1
D4 = 0 - Port A - Output (Direction)
D3 = 0 - Port Cu - Output(Direction)
D2 = 0 - Mode 0
D1 = 0 - Port B - Output (Direction)
D0 = 0 - Port CL- Output (Direction)

5. INTERFACING SWITCHES & LEDS (a) Example Program

- Interfacing — 4 Switches, 4 LEDs (Using 8085 & 8255A)
- Data — from Switches to Display LEDs
- 4 Switches (4 Bit) — Port A (PA_0 -PA_3) – Input to 8085; Logic 0 (off), Logic 1 (on)
- Interfacing LEDs (Logic 0) — Invertor for logic 0 glows LEDs; Port B (PB_0 – PB_3) – Output to LEDs

Program :

```
MVI A 90
OUT 43
IN 40
OUT 41
```

Port A = 40

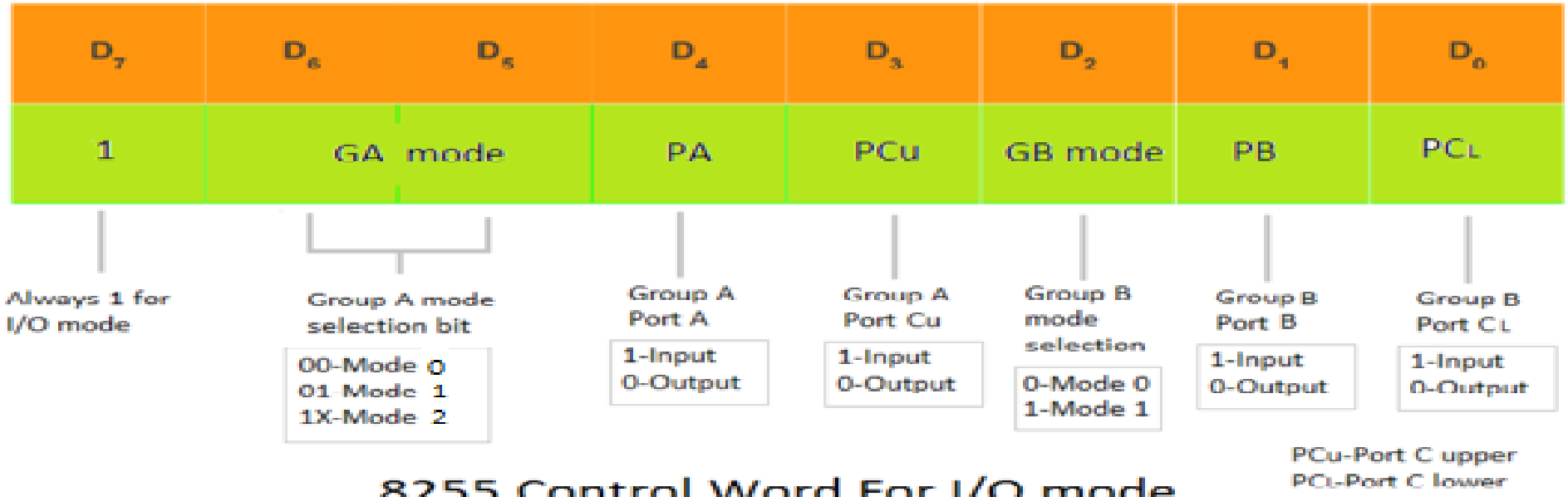
Port B = 41

Port C = 42

Control Register = 43

Port A – Input
Port B - Output
So, Control Word - 90

D7	D6	D5	D4	D3	D2	D1	D0
1	Group A 0 (Mode 0)	0	Port A 1 (Input)	Port Cu 0 (Output)	Group B 0 (Mode 0)	Port B 0 (Output)	Port CL 0 (Output)

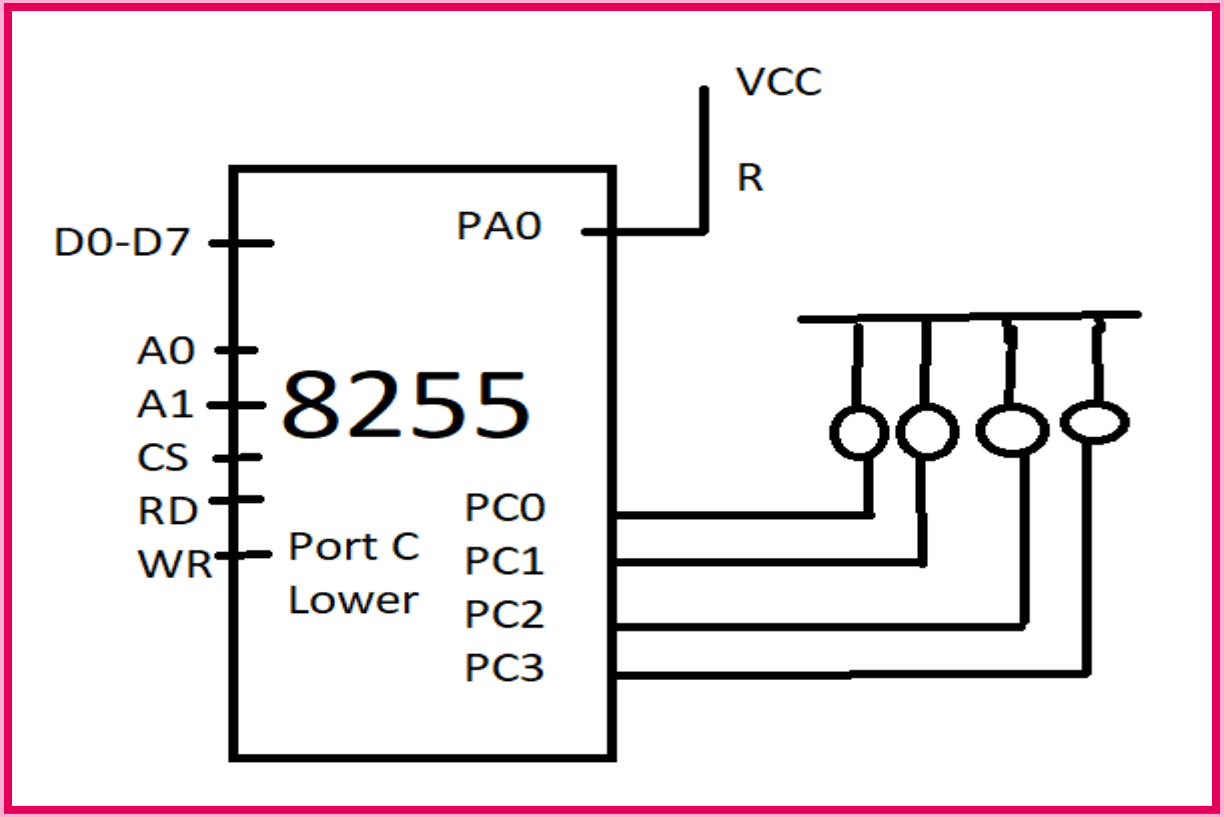


8255 Control Word For I/O mode

5. a . Example Program

Design a system (with Software and hardware) that will cause four LEDs to flash alternately, When a Push Button is Pressed. LSB of PORT A is used for the switch interface and least significant four bits used for PORT C for LEDs Interface.

Solution :



Program :

The Program Check switch Status accordingly makes LED Blink alternately. The data given to PORT C for alternate blink is 0000 1010 (0A) & 0000 0101 (05).

```
        MVI A 90
        OUT  CR
LOOP :  IN PA
        RAR
        JC LOOP
        MVI A, OA
        OUT PC
        CALL DELAY
        MVI A, 05
        OUT PC
        CALL DELAY
        JMP LOOP
```

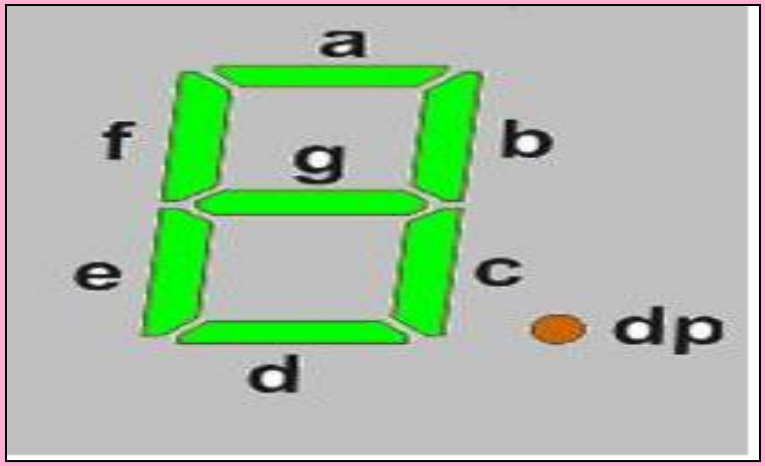
Call Delay Program :

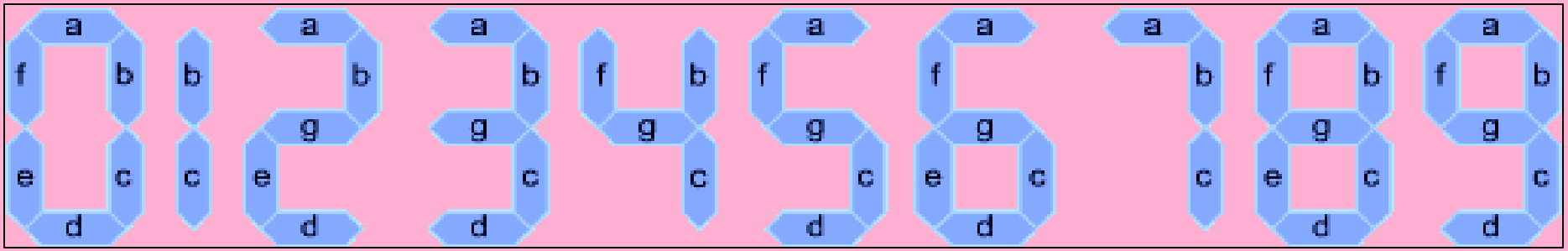
```
DELAY :  LXI B, COUNT
 BACK  :   DCX B
           MOV A,B
           ORA C
            JNZ BACK
            RET
```

6. Interfacing Seven Segment Displays

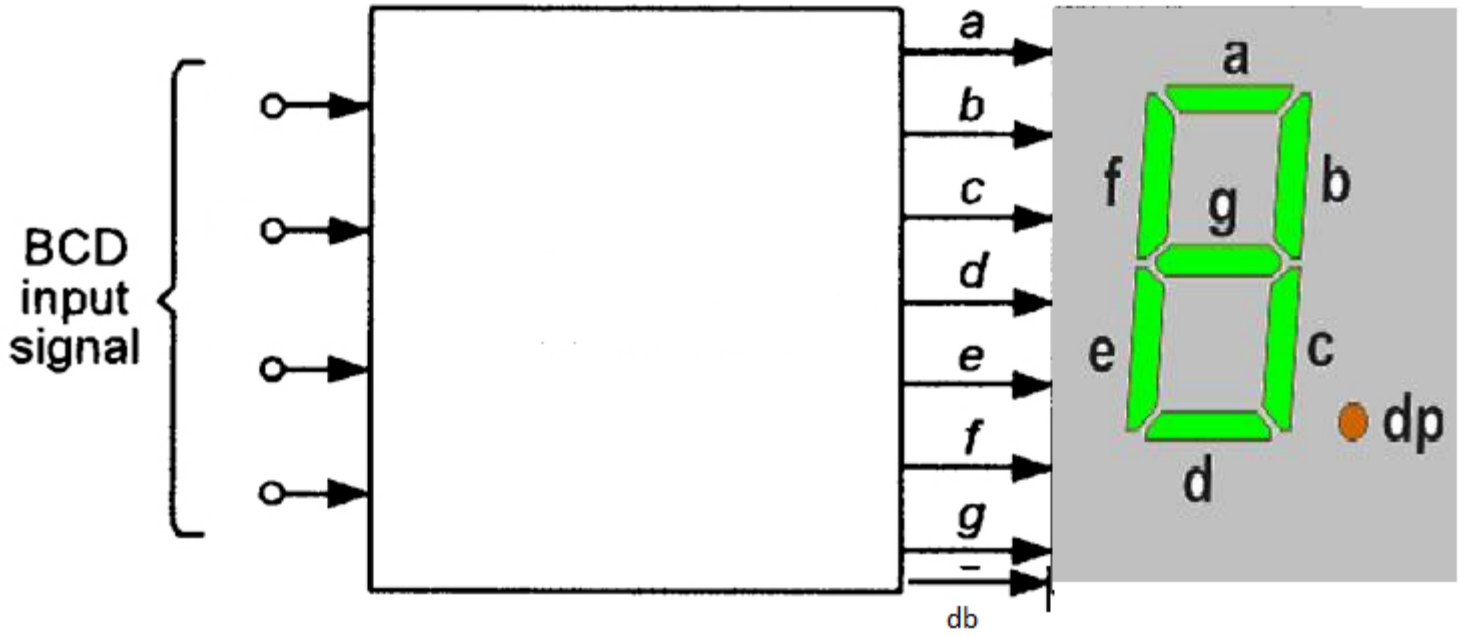
- Seven Segment Display
- Arrangement – Segments for Display - Ten Digits
- Each Segment – Each Pin
- Displays - Common Cathode=1 , Common Anode =0

- BCD to Seven Segment Display Decoder (Driver Circuit)
  (4 Bit Input Pattern required to Display and
  Pattern generated logic 0)





Dig: Arrangement of LED Display



Dig : Driver circuit for single seven segment display

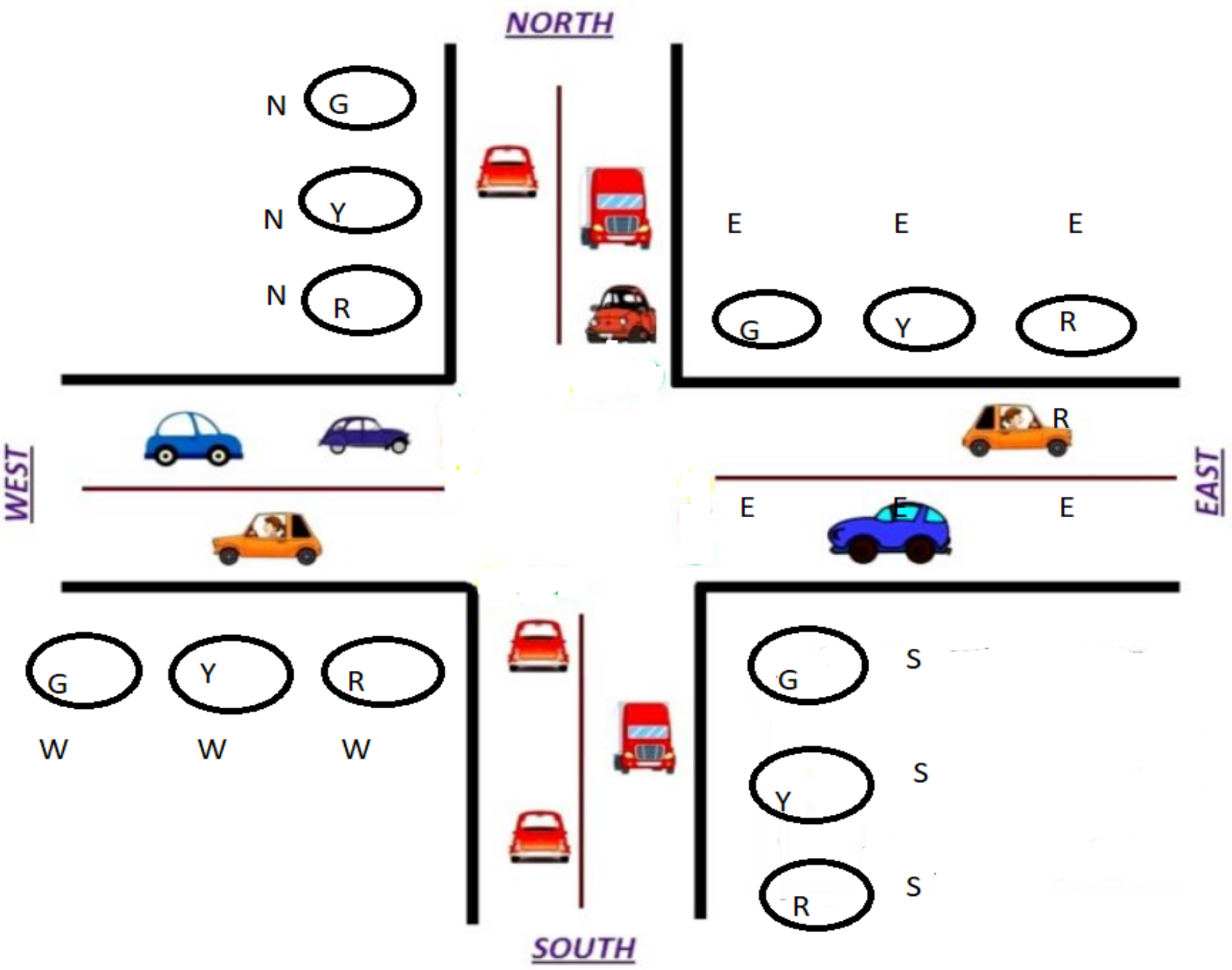
Program :

```
MVI  A  Control Word
OUT  Control Register
MVI  A   Data
OUT  PORT A
```

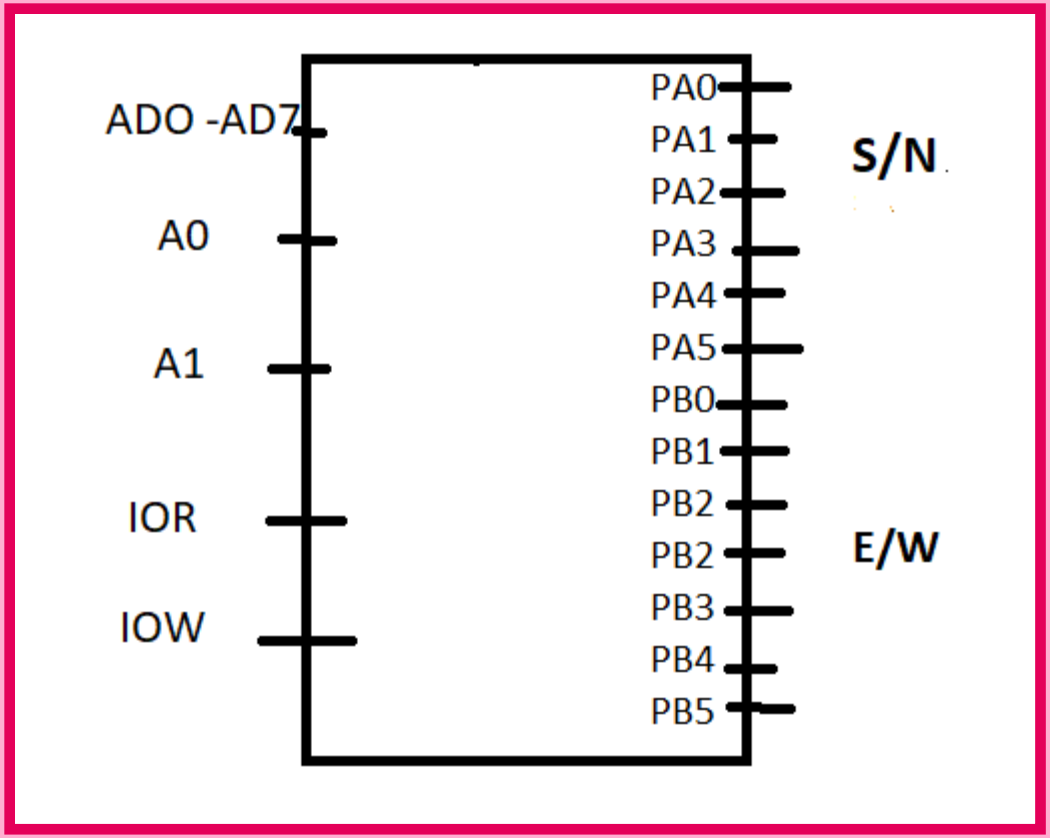
7. Traffic Light Control

Design a Four Road Junction Traffic Control Light System. The Traffic Control sequence as follows

1. **Allow Traffic From the North to other direction.**
2. **Allow Traffic From the East to other direction.**
3. **Allow Traffic From the South to other direction.**
4. **Allow Traffic From the West to other direction.**


NORTH
N G
N Y
N R
E E E
G Y R
R
WEST
EAST
E E E
G Y R
W W W
G S
Y S
R S
SOUTH

- R , Y, G turn on/off
- 230 Volts
- Different RGB (Directions)



Source Program :

The Program given below assume that the 8255 interfaced at the address 80H, 81H, 82H, 83H.

The Data for the port is available at the address 9000H.

The Port data PORT A,PORT B are stored automatically in the starting locations at 9000H.

SEQUENCE	PB7	PB6	PB5 GE	PB4 YE	PB3 RE	PB2 GW	PB1 YW	PB0 RW	PA7	PA6	PA5 GS	PA4 YS	PA3 RS	PA2 GN	PA1 YN	PA0 RN	PORT B DATA	PORT A DATA
NORTH TO OTHER SIDES (GREEN)	X	X	0	0	1	0	0	1	X	X	0	0	1	1	0	0	9	0C
NORTH TO OTHER SIDES(YELLOW)	X	X	0	1	0	0	0	1	X	X	0	0	1	0	1	0	11	0A
EAST TO OTHER SIDES(GREEN)	X	X	1	0	0	0	0	1	X	X	0	0	1	0	0	1	21	9
EAST TO OTHER SIDES(YELLOW)	X	X	0	1	0	0	0	1	X	X	0	1	0	0	0	1	11	11
SOUTH TO OTHER SIDES (GREEN)	X	X	0	0	1	0	0	1	X	X	1	0	0	0	0	1	9	21
SOUTH TO OTHER SIDES (YELLOW)	X	X	0	0	1	0	1	0	X	X	0	1	0	0	0	1	0A	11
WEST TO OTHER SIDES (GREEN)	X	X	0	0	1	1	0	0	X	X	0	0	1	0	0	1	0C	9
WEST TO OTHER SIDES (YELLOW	X	X	0	0	1	0	1	0	X	X	0	0	1	0	1	0	0A	0A

Dig : Traffic Signal control.

Program :

```
START :  MVI A 80
         OUT 83 (CR)

LOOP:    MVI C,08
         LXI H 9000

NEXT :   MOV A, M
         OUT 80 (PA)
         INX H
         MOV A,M
         OUT 81 (PB)
         CALL DELAY
         INX H
         DCR C
         JNZ   NEXT
         JMP   LOOP
```

Delay Subroutine:

```
DELAY :   MVI B, COUNT 1
LOOP 1:   LXI D , COUNT

LOOP 2:   DCX D
          MOV A, D
          ORA E
          JNZ LOOP2
          DCR B
          JNZ LOOP1
          RET
```

Unit - 4

CHAPTER : 8086 MICROPROCESSOR AND ADVANCED MICROPROCESSOR

1. Introduction to 8086 Microprocessor [5 Marks]
2. Architecture of 8086 Microprocessor [10 Marks]
3. Pin Details of 8086 [10 Marks]
4. Advanced Microprocessor [5 Marks]
5. 80186 Architecture [5 Marks]
6. 80286 Architecture [5 Marks]

CHAPTER : PENTIUM MICROPROCESSOR :

7. Architecture of Pentium [10 Marks]
8. Other Versions of Pentium [10 or 5 Marks]
   - i. Pentium Pro Processor
   - ii. Pentium II Processor
   - iii. Pentium III Processor
   - iv. Pentium IV Processor

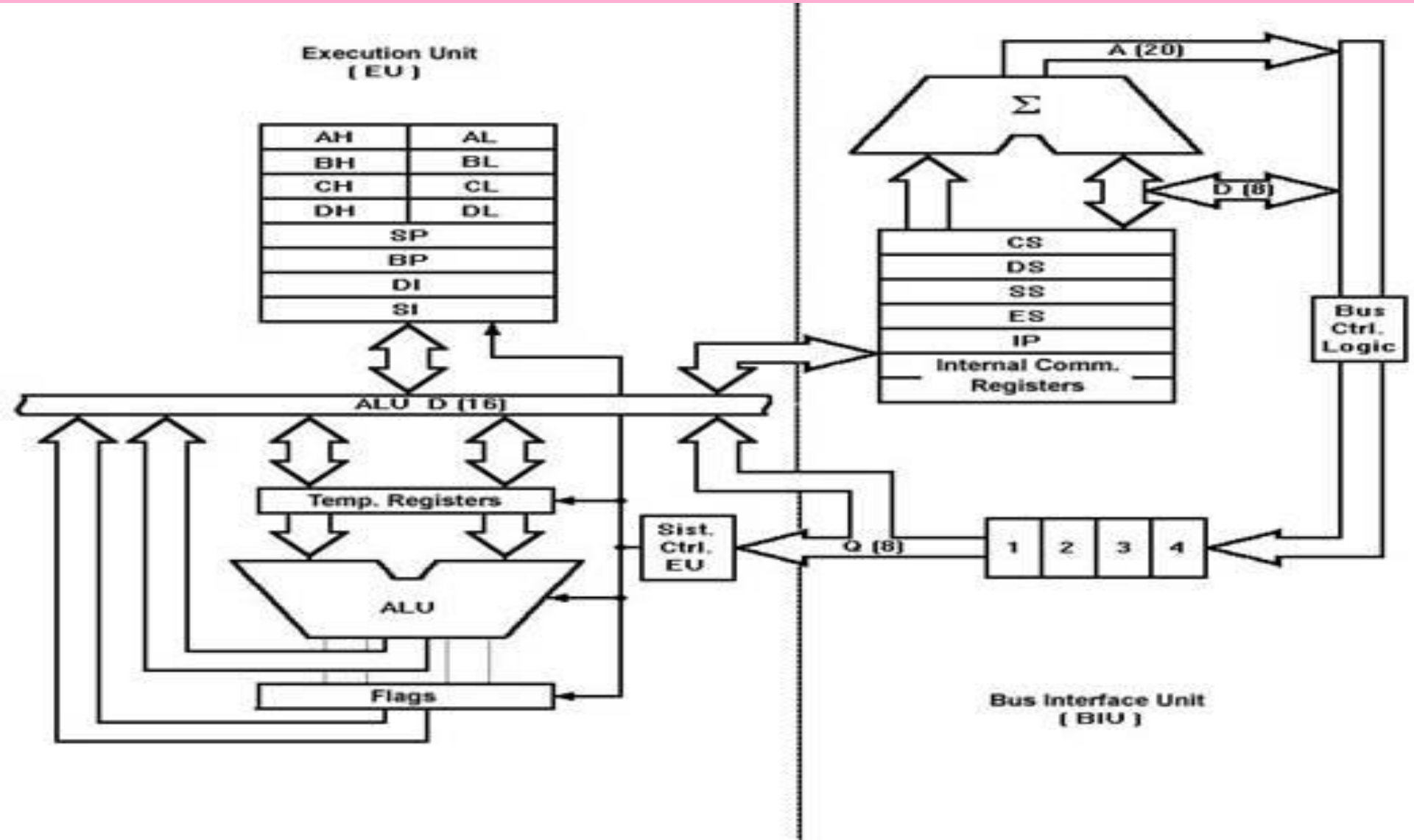
1. Introduction to 8086 Microprocessor

- 16 Bit
- 400 NS
- 25 MIPS
- 1 MB Address
- 20 Bit Address
- Data Bus 16 Bits
- Higher Execution Speed
- Mini Computers
- Six Byte Intruction Queue

2. ARCHITECTURE OF 8086

A. EXECUTION UNIT B. BUS INTERFACE UNIT

Dig : Functional Block Diagram of 8086



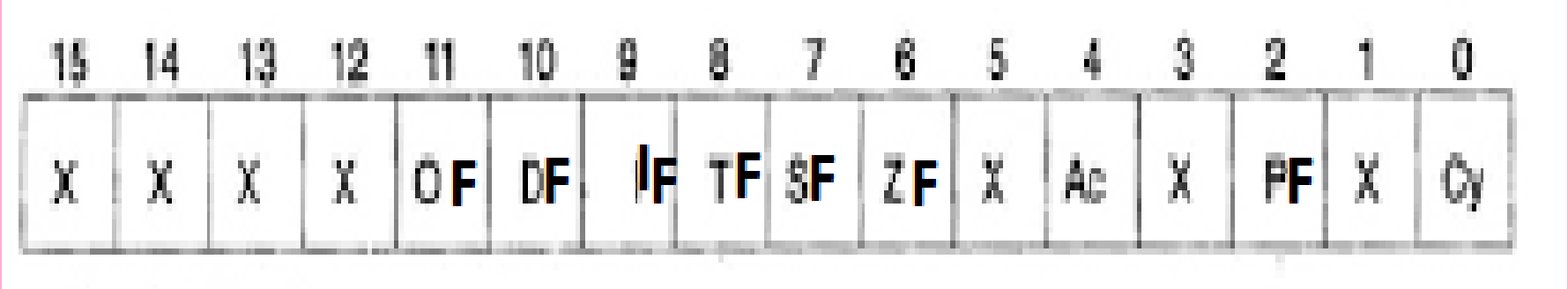
A. EXECUTION UNIT

- ALU
- 16 Bit General Purpose Register
- 16 Bit Flag

- 16 Bit General Purpose Register

AX - AH & AL	AX - Accumulator	SP – Stack Pointer
BX - BH & BL	BX - Data Value	BP - Base Pointer
CX - CH & CL	CX – Count Value	SI - Source Index
DX - DH & DL	DX - Part of Result	DI - Destination Index

❖ 16 Bit Flag



CY - Carry Flag

PF - Parity Flag

AF - Auxiliary Flag

ZF - Zero Flag

SF - Sign Flag

TF- Trap Flag

DF – Direction Flag

IF - Interrupt Flag

OF – Overflow Flag

X – Not Used

B. BUS INTERFACE UNIT

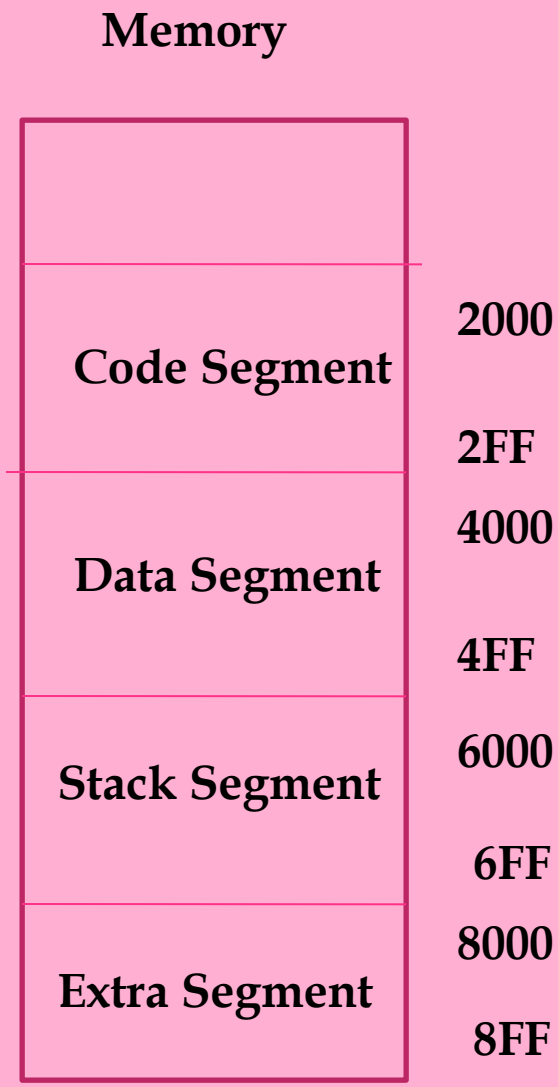
Segment Register (Indicates starting address for different segments in memory)

1. **CS – Code Segment - Program**
2. **DS – Data Segment - Data**
3. **SS - Stack Segment - Stack , Call , Return**
4. **ES – Extra Segment - String**

Example:

Let us assume that the segment Register have following values stored in them.

CS	DS	SS	ES
2000 H	4000 H	6000 H	8000 H



Dig: Memory Location of Different Segments

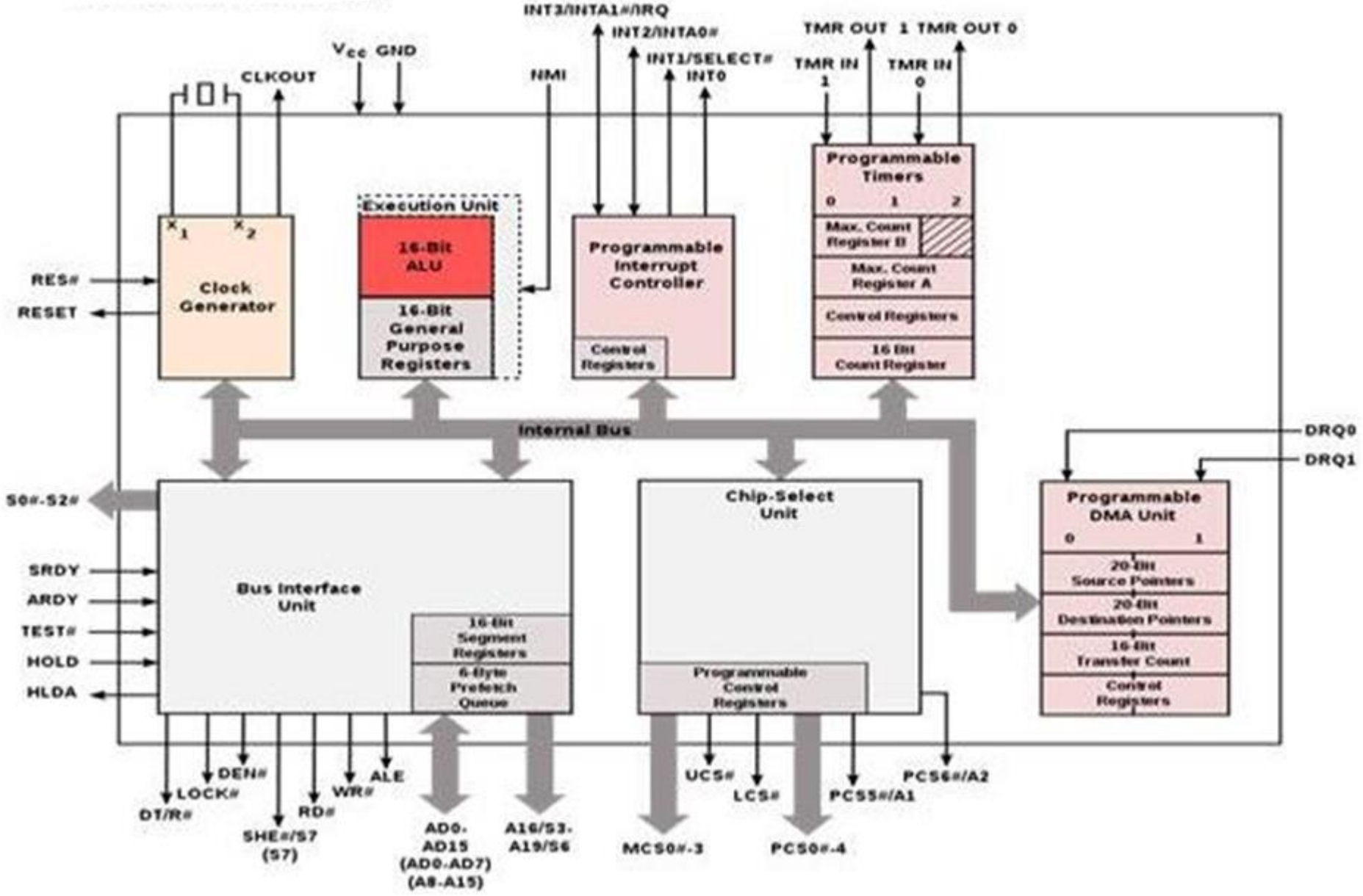
5. 80186 Architecture

- 16 Bit
- 3 Timers (16 Bit Timer)
- 2 DMA operations
- Interrupt Controller
- 68 Pins
- 6,8,12,16,25 MHZ speed
- CG – Clock Generator
- PIC – Program Interrupt Controller
- Chip select unit - M/IO
- Program control Register
- Six Byte Queue

Instructions :

- IN , OUT
- Push n
- Pop n
- Enter
- Leave

80186 architecture:



6. 80286 Architecture

- Protected Virtual address Mode (PVAM)
- 4 level Protection Mechanism

Descriptors

Description Table

Selectors

Task Management

80286 divided into following parts,

a. Bus Unit

b. Instruction Unit

c. Execution Unit

d. Address unit.

a. Bus unit:

A/D latches
R/W
Transfer data

b. Instruction Unit :

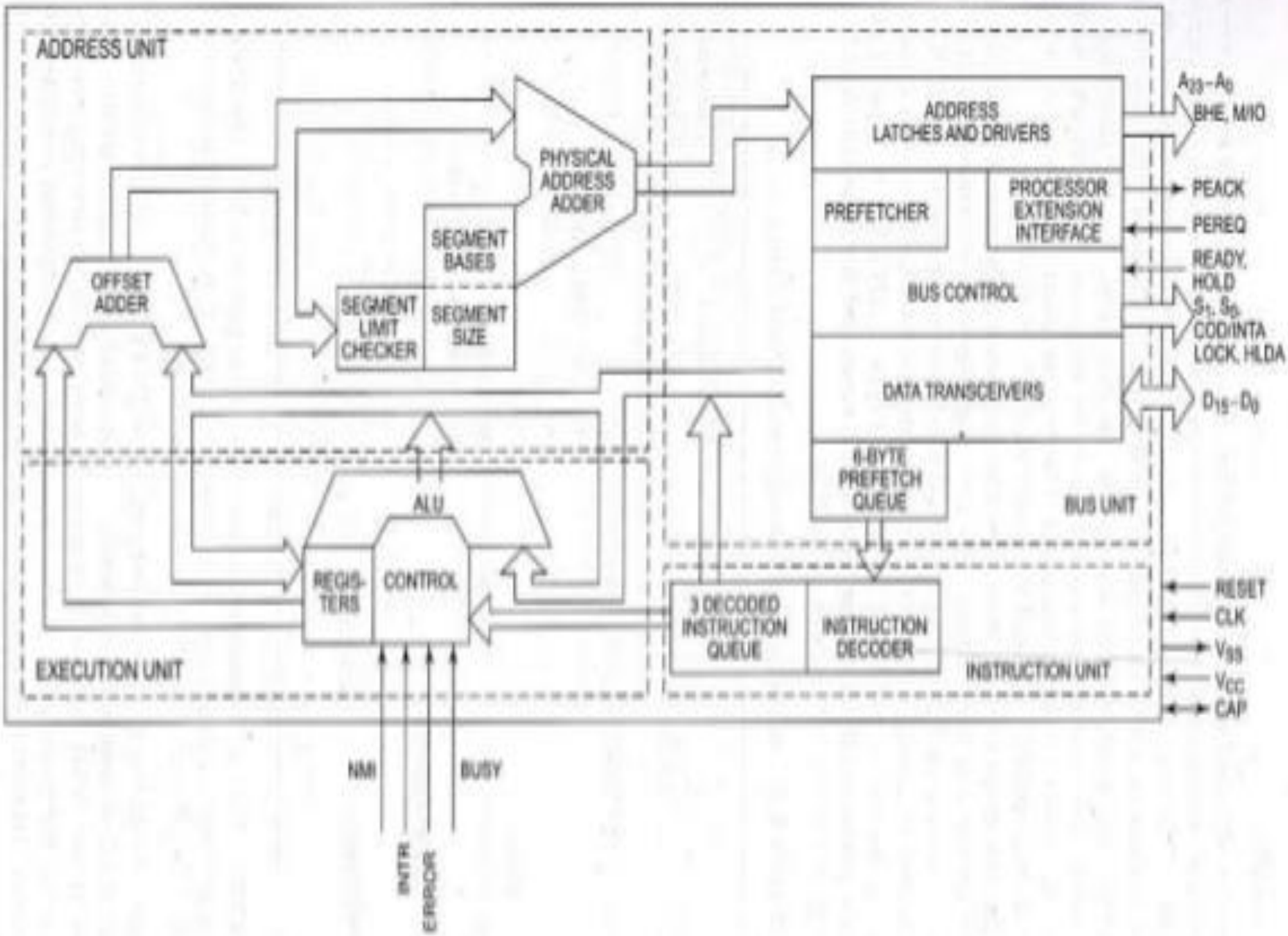
holds the instructions in Queue
decoded

c. Execution Unit:

16 Bit ALU
Execute the instruction

d. Address Unit:

Memory Related task



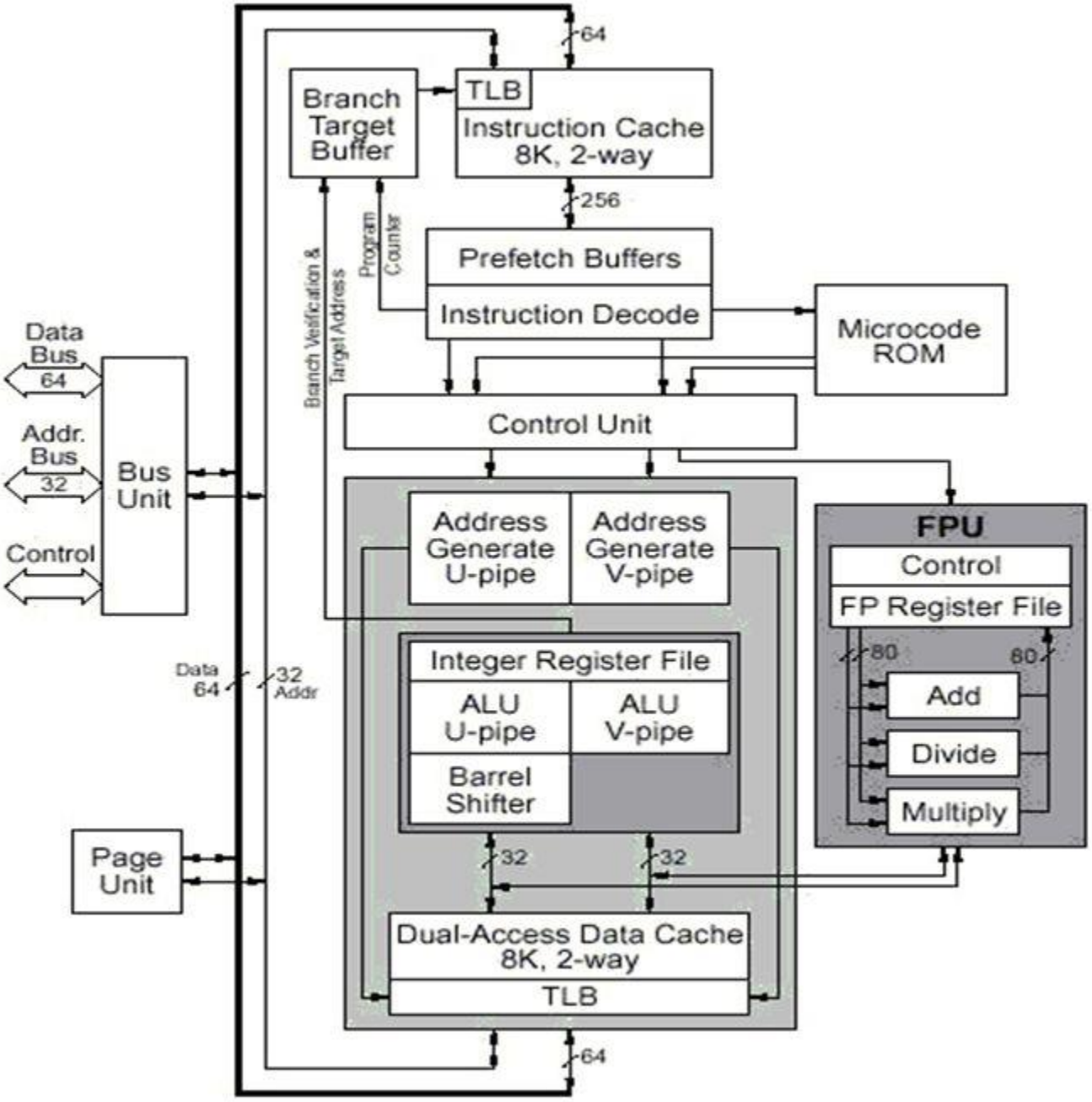
80286 Architecture

7. Architecture of Pentium

- 32 Bit Address
- 80586
- 1993
- Complex Instruction set Computers (CISC)
- Bipolar Complementary oxide semiconductor (BICMOS)
- 273 Pin
- 64 Bit data bus
- 8 KB cache - 4 kb - Code , 4 kb – data
- Each cache – separate address

  Translation Latch Buffer (TLB)

  Simultaneous access data and code.



Dig : Block Diagram of Pentium

- **Integer Pipeline U & V,**

  U-Pipeline, V- Pipeline

- **5 Stages of Integer Pipeline**

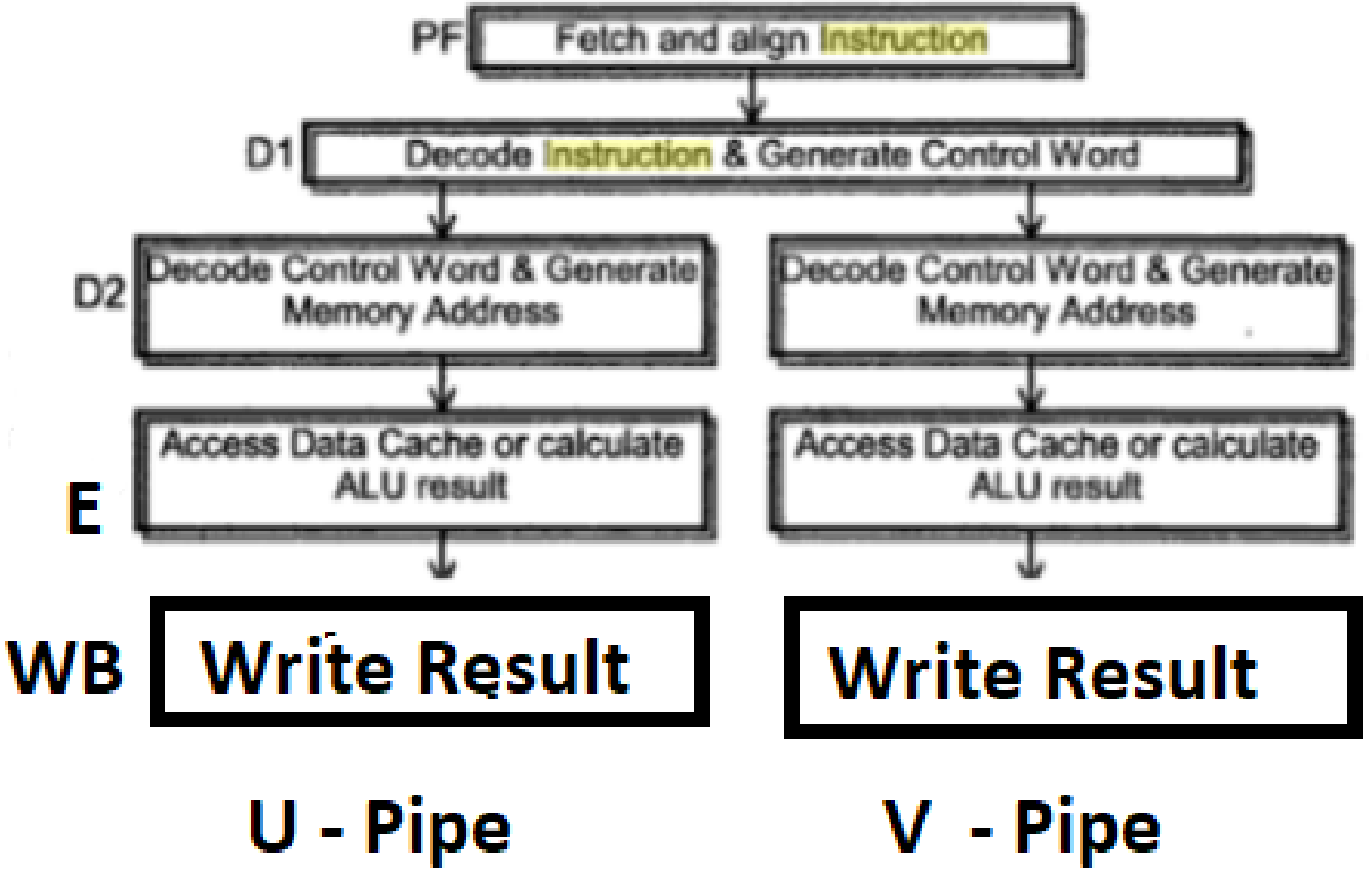
  a. PF - Prefetch Code

  b. D1 - Decode – Control word (First decode)

  c. D2 – Decode Next Control Word (Second decode)

  d. E - Execute (ALU)

  e. WR – Store the result (Write Back)



Dig: Integer Pipeline Stages in the Pipeline

❖ Floating Point Pipeline (FPU Pipeline),

PF	D1	D2	E	X1	X2	WF	ER

8 Stages of FPU Pipeline

1. PF - Prefetch Code
2. D1 - Decode – Control word (First decode) – Same as Integer Pipeline
3. D2 – (Second decode)
4. E - Operand Fetch (Operands Fetches from cache)
5. X1 - (First Execute) - 1 step Execute
6. X2 - (Second Execute) – 2 Step Execute
7. WF - (Write Float) - Wait Result
8. ER - (Error Report) - When Fails

8. Other Versions of Pentium

a) Pentium Pro

b) Pentium II

c) Pentium III

d) Pentium IV

a) Pentium Pro

- P6
- 21 Million Transistors
- 3 Integer Units
- FPU Performance high
- 150 Mhz and 166 Mhz
- 16 KB – 8KB data , 8 KB code
- 3 Execution Engine – 3 Instructions Parallel (no Conflict)
- 32 Bit Data
- 4 GB Memory , 64 GB Memory (36 Address Bus)

B. Pentium II

- 1997
- Integrated Circuits
- 66 Mhz or 99 Mhz (Cache Operation)
- 133 Mhz
- 512 Kb Memory
- MMX Pentium Pro (Multimedia Extensible)
- Bus Speed 66 Mhz , 100 Mhz, 360 Mhz, 400 Mhz, 450 Mhz
- SDRAM

C. Pentium III

- Plastic Catridge
- Clock Frequency - 1GHz
- 66 Mhz or 99 Mhz (Cache Operation)
- I Version – 512 Cache
- II Version – 256 Cache
- Flipchip
- Memory Speed 100 Mhz
- Bus Speed - 100 Mhz to 133 Mhz

C. Pentium IV

- 2000
- P4 available : 1.3 Ghz ,1.4Ghz ,1.5 Ghz Speed
- 66 Mhz or 99 Mhz (Cache Operation)
- RAM , SDRAM
- Higher Speed
- 8 KB cache (L1) , 32 KB cache (L1), 256 KB Cahe (L2)
- Bus Speed - 133 Mhz to 200 Mhz

- 2000
- P4 available : 1.3 Ghz ,1.4Ghz ,1.5 Ghz Speed
- 66 Mhz or 99 Mhz (Cache Operation)
- RAM , SDRAM
- Higher Speed
- 8 KB cache (L1) , 32 KB cache (L1), 256 KB Cahe (L2)
- Bus Speed - 133 Mhz to 200 Mhz

Unit - 5

Chapter : 8051 MICROCONTROLLER

1. Introduction to 8051 Microcontroller [5 Marks]
2. Intel MCS51 series Microcontrollers [5 Marks]
3. Intel 8051 Architecture [10 Marks]
4. Memory Organization [5 Marks]
5. Internal RAM Structure [10 Marks]
6. Power Control in 8051 [5 Marks]
7. Stack Operation [5 Marks]

1. Introduction to 8051 Microcontroller

- Microprocessor - Processor Chip
- Processor Chip classified as

  a) General Purpose MUP

  b) Microcontroller

  c) DSP Processor

a) General Purpose Microprocessor (GPU)

- Digital Computers
- Memory & I/O External Components
- 8085, 8086…….Pentium

B . Microcontroller

- Microcontroller - Machine control chip

  - no need to change the Program

- Equipments to Control :

  Eg: Printers, Plotters, Xerox Machine, telephone,

  Automobile Engine Washing Machine etc.

- Memory
- I/O Ports
- Single Chip , Computer on Chip , System on a Chip
- Faster , reduce work
- 80311, 8051,8096 Microcontrollers

c) DSP Processor

- Mobile Phones
- Flexible hardware / Software
- ALU , FPU

2. Intel MCS-51 Series Microcontrollers

- Microcontroller - 8 Bit and 16 Bit Configuration
- 8 Bit - available many numbers – ie: MCS–51 Series
- Fig 1: shows various microcontrollers in MCS51 series. with their differences.
  - 8XC51RD – Internal ROM 64KB ,
  - 8XC51FC - Internal ROM 32KB

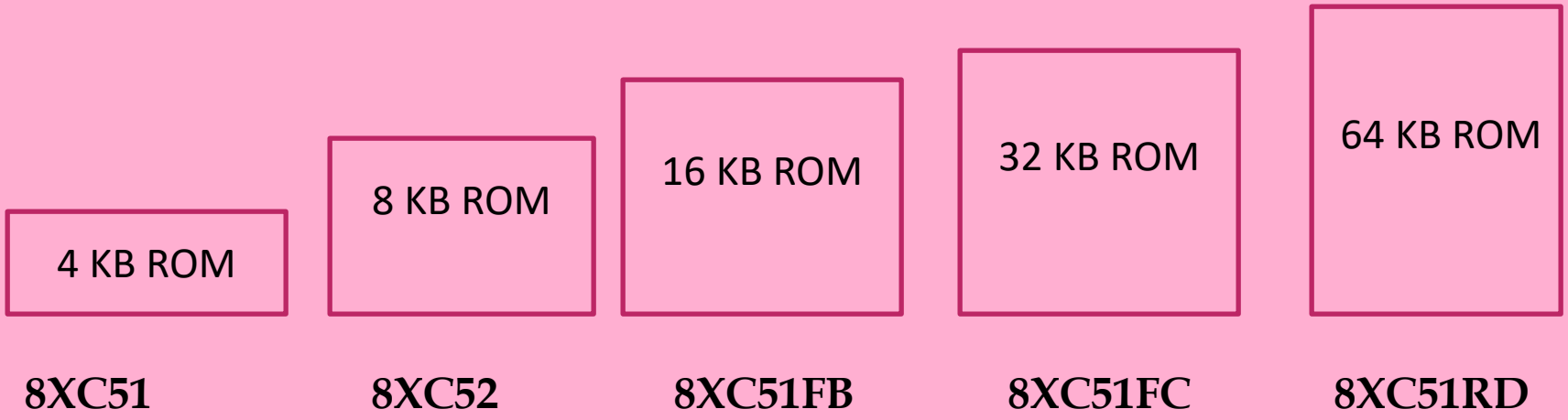


Fig 1 : Microcontroller in Intel MCS-51 Series

❖ **Fig 2 shows the list of features of 8051 family Microcontrollers**

Device Number	Data Bus Width	RAM Capacity	ROM Capacity
8031	8	128	Nil
8051	8	128	4KB
8751H	8	128	4KB - EPROM
8052AH	8	256	8KB
87528H	8	256	8 KB - EPROM

Fig : Features of 8051 family Microcontrollers

3. Intel 8051 Architecture

- 8 Bit ; 4 KB – Program Memory
- 128 Bytes RAM
- 4 Ports – 8 Bits each. (0,1,2,3)
- Port 0 & Port 2 – Multiplex address / Data Bus
- Two 16 Bit Timer
- Full Duplex
- Boolean Processing
- 16 Bit Addressing (Low Order – Multiplex)
- 40 Pins
- Vcc – Power Supply ; Vss – Ground
- 4 Signal (PSEN, ALE, EA, RST) – Conjuction with External Memory.
- XTAL 1, XTAL2 – Crystal

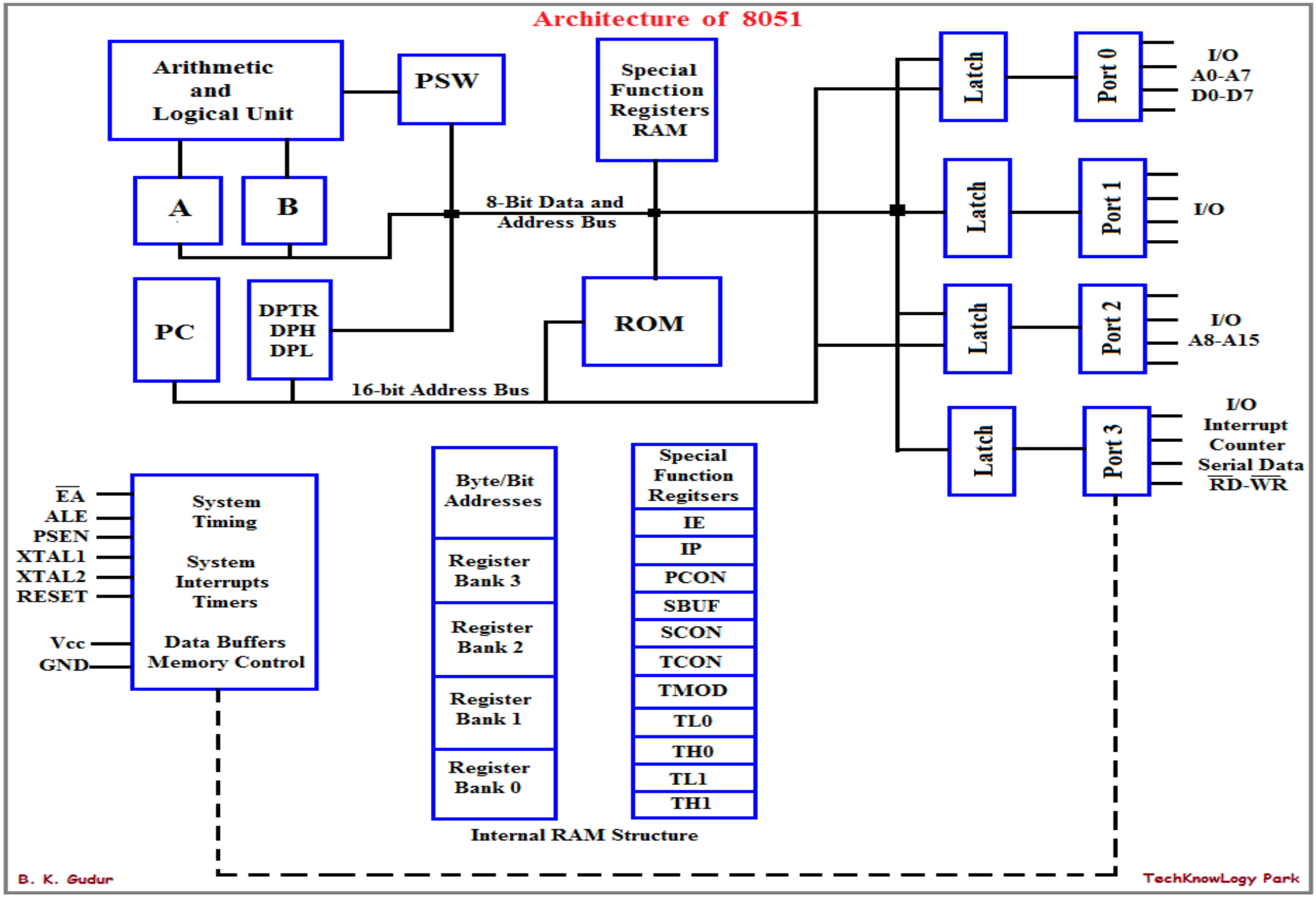


Fig 1 : Intel 8051 Architecture

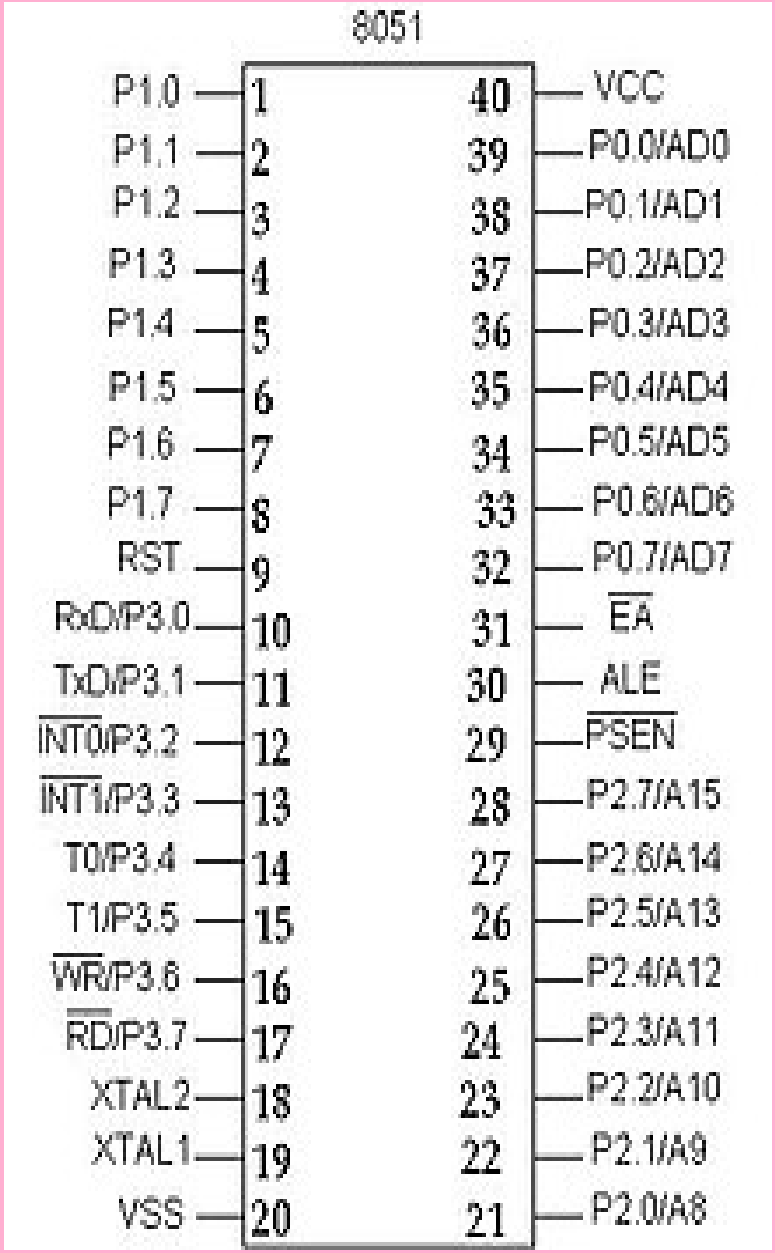


Fig 2 : 8051 Pin Details

4. Memory Organization

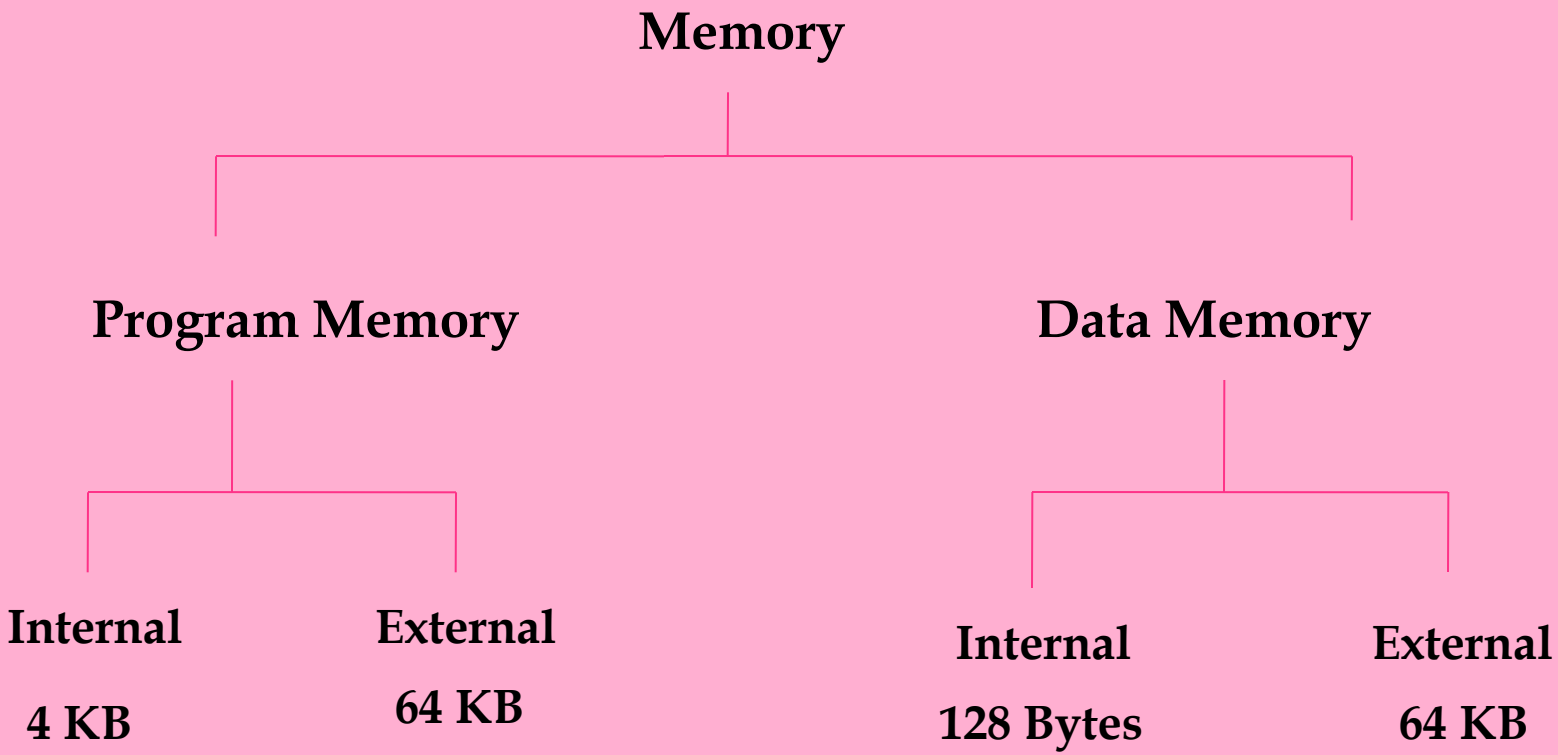


Fig: Memory Organization in 8051

1. **Program Memory**

   a. **Internal**

      - 4KB

   b. **External**

      - 64 KB

   - 16 Bit Address
   - 8 Bit Data

2. **Data Memory**

   a. **Internal**

      128 bytes

   b. **External**

      64 KB

   - 16 Bit Address
   - 8 Bit Data

5. Internal RAM Structure

1. Special Function Register.
2. Processor Status Word.

- 128 Bytes (access Bytes or Bit)
- Dig: Internal RAM
- Store 00H to 7F
- Divided Space - 3 Blocks. a. Register Banks
  b. Bit Addressable Memory
  c. Scratch Pad Memory

a. Register Bank

- 4 Banks of 8 Register (00 to 1F)
  - Bank 0 = 00-07
  - Bank 1 = 08-0F
  - Bank 2 = 10-17
  - Bank 3 = 18-1F

a. **Bit addressable Memory**

- **Bit Wise Operation**
- **(07 to 7F)**

b. **Scratch Pad Memory**

- **Read / Write Operation and other Purposes**
- **(30 to 7F)**

a. Special Function Register.

- Access by Direct Addressing
- Occupy with in 128 Bytes

The Registers are

1. Accumulator A& B
2. Processor Status Word (PSW)
3. I/O Port Register - P0,P1,P2,P3
4. Data Pointers – DPH & DPL
5. Serial data buffer Register – SBUF
6. Stack Pointer – SP
7. Timer Register - THO , TH1 and TLO, TL1
8. Timer Control Register - TCON and TMOD
9. Power and Port Control - PCON and SCON
10. Interrupt Register - IP and IE

Table : Special Function Register.

Name of the Register	*Internal RAM Address (HEX)*
ACC	E0H
B	F0H
DPH	83H
DPL	82H
IE	A8H
IP	B8H
P0	80H
P1	90H
P2	A0H
P3	B0H
PCON	87H
PSW	D0H
SCON	98H
SBUF	99H
SP	81H
TMOD	89H
TCON	88H
TL0	8AH
TH0	8CH
TL1	8BH
TH1	8DH

b. Processor Status word [PSW]

PSW	CY	AC	F0	RS1	RS0	OV	-	P
Bit address	D7H	D6H	D5H	D4H	D3H	D2H	D1H	D0H
Contents upon Reset	0	0	0	0	0	0	0	0

1. **P- Parity Bit :** 1- odd , 0 Even

2. **OV – Overflow :**

+ve	+	+ve	=	-
- ve	+	-ve	=	+
+ve	-	-ve	=	-
-ve	-	+ve	=	+

3. **Register Select (RSO & RS1) :**

RS1	RS0	SELECTED BANK	ADDRESS RANGE
0	0	Bank 0	00H – 07H
0	1	Bank 1	08H - OFH
1	0	Bank 2	10H- 17H
1	1	Bank 3	18H – 1FH

4. **FO : -** Store any bit
5. **AC : -** Auxillary Carry
6. **CY –** Carry Flag

I. Accumulator :

A & B

A- Add ,Sub

B – Mul , Div

Accumulator Bits	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0
Bit address	E7	E6	E5	E4	E3	E2	E1	E0
Contents upon Reset	0	0	0	0	0	0	0	0

Table 1: Addresses & Contents of Accumulator A Bits

Accumulator Bits	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0
Bit address	F7	F6	F5	F4	F3	F2	F1	F0
Contents upon Reset	0	0	0	0	0	0	0	0

Table 2: Addresses & Contents of Accumulator B Bits

6. Power Control in 8051

- Various power control mode in 8051
- Power Control mode selected through SFR (PCON)

Bit	Name	Function
7	SMOD	Serial Port
6	-	RESERVED
5	-	RESERVED
4	-	RESERVED
3	GF1	General Purpose Flag 1
2	GF)	General Purpose Flag 0
1	PD	Power Down Mode Set Bit
0	IPL	Idle mode set bit

Table : Bit Pattern of PCON Register

a. Idle Mode :

- PCON - set 0
- Interrupt Controller Active
- CPU not affected contents
- Processor revoked active .

b. Power Down Mode :

- PCON - set 1
- Clock generator Switched off
- Reduce 2V
- Power Down
- Reset - Revoke

7. Stack Operation :

- Series of Memory Location
- LIFO
- Stack Initialized – Internal RAM area
- 8 Bit Stored
- SP in SFR used to intialized the stack .
- SP use by SFR direct address as 81
- PUSH
- POP
- PUSH – SP Incremented
- POP – SP decremented

- **Other Stack operation**

  ACALL

  LCALL

  RET

- **SP intilized by SFR in Internal RAM area by Programmer**